

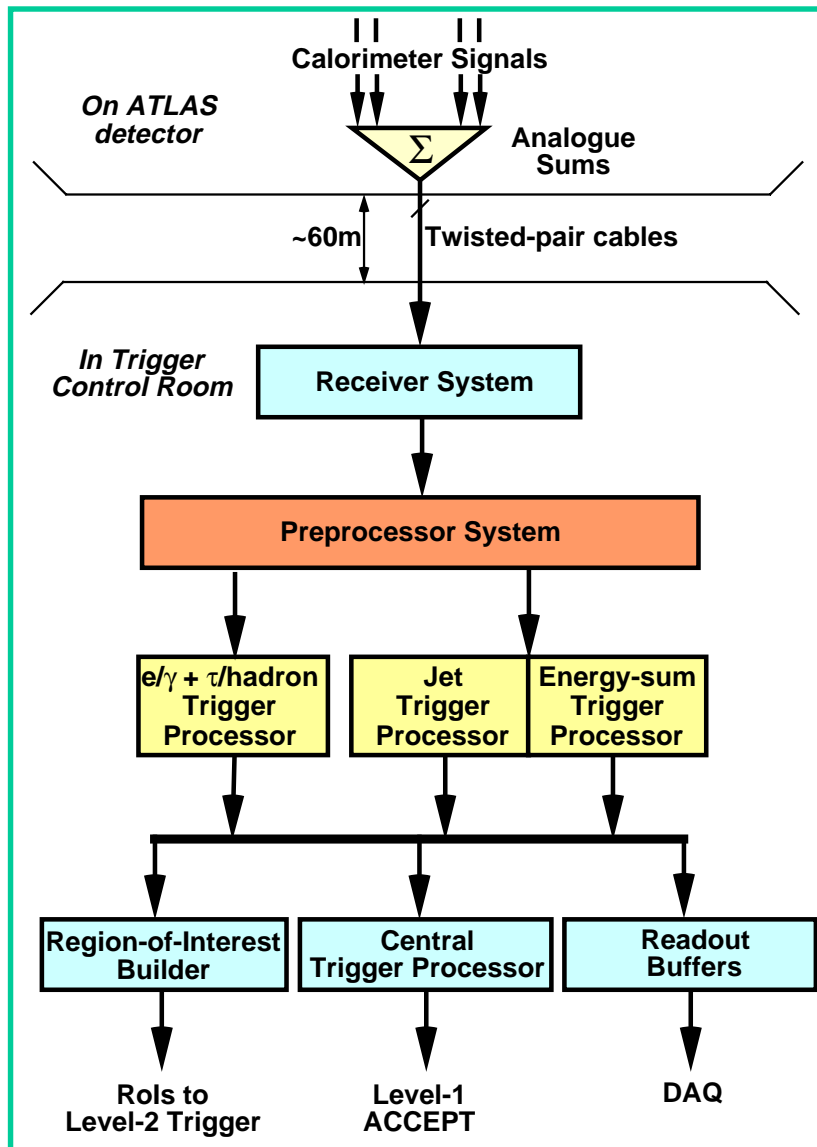


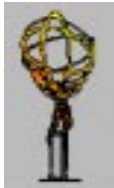
ASSO - Level-1 Calorimeter Trigger *Cluster and Jet/Energy Processors*



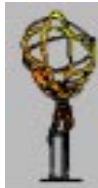
- **Overview**
- **Deliverables**
- **Programme organisation**
- **Infrastructure**
- **Interfaces - Input**
- **Interfaces - Output**
- **Schedule - Milestones**
- **Quality Assurance**
- **Recent results**

ASSO - Level-1 Calorimeter Trigger Overview





ASSO - Level-1 Calorimeter Trigger *Deliverables - (1)*

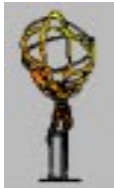


- **Cluster Processor:**

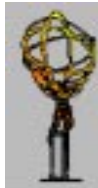
- searches for signatures of high- p_T e/γ and τ /hadrons
- calculates total multiplicity of e/γ and τ /hadron “objects”
- provides Region of Interest (RoI) information to Level-2 Trigger
- monitors incoming and outgoing data from Level-1 ACCEPTs (to DAQ)

- **Jet/Energy Processor:**

- searches for signatures of high- E_T jets
- calculates total multiplicity of jets and forward jets
- calculates missing E_T , total scalar E_T (*and total jet E_T*)
- provides Region of Interest (RoI) information to Level-2 Trigger
- monitors incoming and outgoing data from Level-1 ACCEPTs (to DAQ)



ASSO - Level-1 Calorimeter Trigger *Deliverables - (2)*

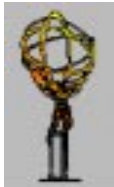


- **Hardware:**

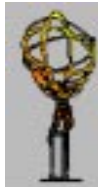
- **Cluster Processing Module (CPM) ~65 modules**
- **Jet/Energy Module (JEM) ~40 modules**
- **Common Merger Module (CMM) ~15 modules**
- **Timing Control Module (TCM) ~20 modules**
- **ReadOut Driver module (ROD) ~25 modules**
- **Processor Backplane (PB) ~10 boards**
- **Serial Link cable system ~2000 cables**
- **9U VME crates (commercial) ~10 crates**
- **VME Processor (commercial) ~10 modules**

- **Software:**

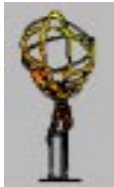
- **Control, monitoring, diagnostics and associated DAQ infrastructure**



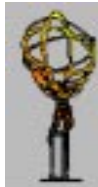
ASSO - Level-1 Calorimeter Trigger Programme Organisation



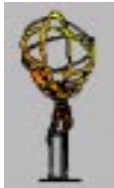
- **Cluster Processor - UK (18.7 FTE)**
 - **CPM (hardware) - Birmingham University**
 - **Algorithms/Software - Birmingham University, QM London, RAL**
- **Jet/Energy Processor - Germany and Sweden (5.0 FTE)**
 - **JEM (hardware) - University of Mainz**
 - **Algorithms/Software (Jet triggers) - University of Stockholm**
 - **Algorithms/Software (Energy triggers) - University of Mainz**
- **“Common” items**
 - **CMM - RAL**
 - **TCM - RAL**
 - **ROD - RAL**
 - **PB - University of Stockholm**
 - **Serial Link cable system - CP/JEP Institutes (shared responsibility)**



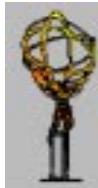
Atlas Level-1 Calorimeter Trigger Infrastructure (1)



- **Cluster Processor & “Common” Modules:**
 - **Schem capture/layout (*in-house*):** CADENCE v13.5 (*moving to v14.0 <2002*)
 - **Firmware (*in-house*):**
 - FPGA ADVANTAGE v5.1 (*HDS, Leonardo Spectrum, ModelSim*)
 - Xilinx ISE v4.1
 - Altera MAX+PLUS II
 - **Manufacturing (*out-sourced*):** Commercial
 - **Testing (*in-house*):**
 - JTAG
 - Xilinx Chip-Scope
 - Module stand-alone → CP sub-system
 - **Integration (*Heidelberg + CERN*):** Full Level-1 “Slice” tests → ATLAS



Atlas Level-1 Calorimeter Trigger Infrastructure (2)



- **Jet-Energy Processor:**

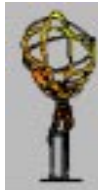
- **Schem capture/layout (*in-house*):** CADENCE v13.6
- **Firmware (*in-house*):** FPGA ADVANTAGE
Xilinx Foundation v3.3i
- **Manufacturing (*out-sourced*):** Commercial
- **Testing (*in-house*):** Module stand-alone → JEP sub-system
- **Integration (*Heidelberg + CERN*):** Full Level-1 “Slice” tests → ATLAS

- **Backplane:**

- **Schem capture/layout (*in-house*):** Mentor Graphics design suite
- **Manufacturing (*out-sourced*):** Commercial (APW)
- **Testing (*in-house*):** Board stand-alone → CP/JEP sub-systems



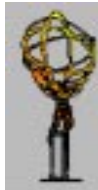
Atlas Level-1 Calorimeter Trigger *Interfaces - Input*



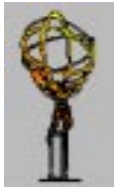
- **Real-time data path:**
 - ~2000 cables carrying serial LVDS data at 480 Mbaud/channel from PPr system
 - *Ref:* wwwasic.kip.uni-heidelberg.de/atlas/L1/DISCUSS/PPMod_Spec_PostPDR_1.pdf
 - *Contact:* P Hanke (KIP, University of Heidelberg)
- **TTC timing/control path:**
 - ~7 optical fibres from TTC system into TCMs (*1 TCM per crate*)
 - *Refs:* ATLAS DAQ-98-103
<http://ttc.web.cern.ch/TTC/intro.html>
 - *Contacts:* P Gallno, P Farthouat
- **Detector Control System:**
 - CAN-bus for monitoring
 - *Contact:* H Burckhart



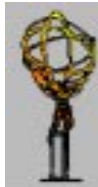
Atlas Level-1 Calorimeter Trigger *Interfaces - Output*



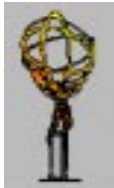
- **Real-time data path:**
 - **Multiplicities of e/γ and τ /hadron clusters and jets, and missing/total energy sums to CTP**
 - **Ref: CTP Technical Specification (*ATL-DA-ES-0006*)**
 - **Contact: R Spiwoks, Y Ermoline**
- **RoI data to Level-2:**
 - **6 S-link fibre-pairs (160 Mbyte/s) to RoIB**
 - **Ref: Specification of the LVL1/LVL2 trigger interface (*ATL-D-ES-0003*)**
 - **Contact: J Dawson, Y Ermoline**
- **“Slice” data to DAQ:**
 - **12 S-link fibre-pairs (160 Mbyte/s) to ROS**
 - **Contact: D Francis**



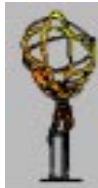
Atlas Level-1 Calorimeter Trigger Schedule - Milestones



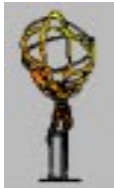
<i>PBS no</i>	<i>Milestone</i>	<i>Date</i>
10.1.2.1	Start CP/JEP sub-system tests	Jan 2002
10.1.2.1	Start "Slice" tests	April 2002
10.1.2.1	Completion of "Slice" tests ($\phi 1$)	July 2002
10.1.2.1.4.8	FDR for TCM	Oct 2002
10.1.2.1.4.8	PRR for TCM	Nov 2002
10.1.2.1.4.9	PDR for ROD (CP/JEP)	Oct 2002
10.1.2.1.4.3	FDR for Processor Backplane (PB)	Oct 2002
10.1.2.1.2.1	FDR for CPM	Nov 2002
10.1.2.1.4.3	PRR for Processor Backplane (PB)	Nov 2002
10.1.2.1.2.1	PRR for CPM	Dec 2002
10.1.2.1.3.1	FDR for JEM	Dec 2002
10.1.2.1.3.1	PRR for JEM	Jan 2003
10.1.2.1.4.1	FDR for CMM	Jan 2003
10.1.2.1.4.1	PRR for CMM	Feb 2003
10.1.2.1	Completion of "Slice" tests ($\phi 2$)	April 2003
10.1.2.1.4.9	FDR for ROD (CP/JEP)	Jun 2003
10.1.2.1.4.9	PRR for ROD (CP/JEP)	Jul 2003
10.1.2.1.2	Full CP sub-system available for System tests	Dec 2003
10.1.2.1.3	Full JEP sub-system available for System tests	Jan 2004
10.1.2.1.2	Completion of CP sub-system tests	Dec 2004
10.1.2.1.3	Completion of JEP sub-system tests	Jan 2005
10.1.2.1	Calorimeter trigger available in situ	May 2005



Atlas Level-1 Calorimeter Trigger *Quality Assurance*

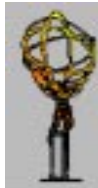


- **3-level review system:**
 - Every major component/module subject to PDR/FDR process, followed by PRR
 - PRR (*with TC representative from FDR*) to approve full manufacture
- **All UK electronics will conform to ISO9000 procedures:**
 - PCB manufacturers do “Flying-Lead” **bare-board tests** (*net-list*) & **Z₀ tests**
 - **Route Cards and Problem Reports** for all modules, from delivery of bare PCBs
 - Assembly companies (*also ISO9000-compliant*) will run small pre-production batches to set up **soldering temperature profiles**, etc
 - **Visual inspection** of assembled boards first at assembly company, then at RAL
 - Assembled boards subject to pre-defined **Test Plan** - initially **JTAG**
 - Route Cards updated with specific faults
 - Problem Reports catalogue a compilation of generic faults

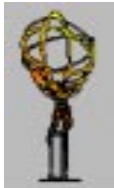


Atlas Level-1 Calorimeter Trigger

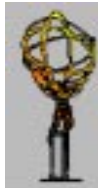
Recent Results (1)



- **LVDS tests (Birmingham/Mainz):**
- Trigger uses ~7000 high-bandwidth serial links (e.g. >4 Gbyte/s → CPM)
- Bit-error rate (BER) requirements <math><10^{-10}</math> per link (to minimise false triggers)
- NS Bus LVDS (de)serialiser chipset - DS92LV1021/121
- Studied cable types, lengths (<math><20\text{m}</math>), pre-compensation techniques
- BER <math><10^{-13}</math> per link achieved for cable lengths up to 20m (L-R equalisation)
- N.B. Important requirements (achievable):
 - good board layout, clean power supplies, low clock jitter, ...



Atlas Level-1 Calorimeter Trigger *Recent Results (2)*



- **ROD tests (CERN):**
- **TTC used to trigger system**
- **Rols sent on G-link to ROD**
- **Fragments sent in parallel to RoIB/ROS**
- **Fragments fully-checked on receipt**
- **Firmware errors in S-Link interfaces (*now understood*)**
- **ROD latency within specifications ($\ll 10 \mu\text{sec}$)**

