CP chip tests using GTM

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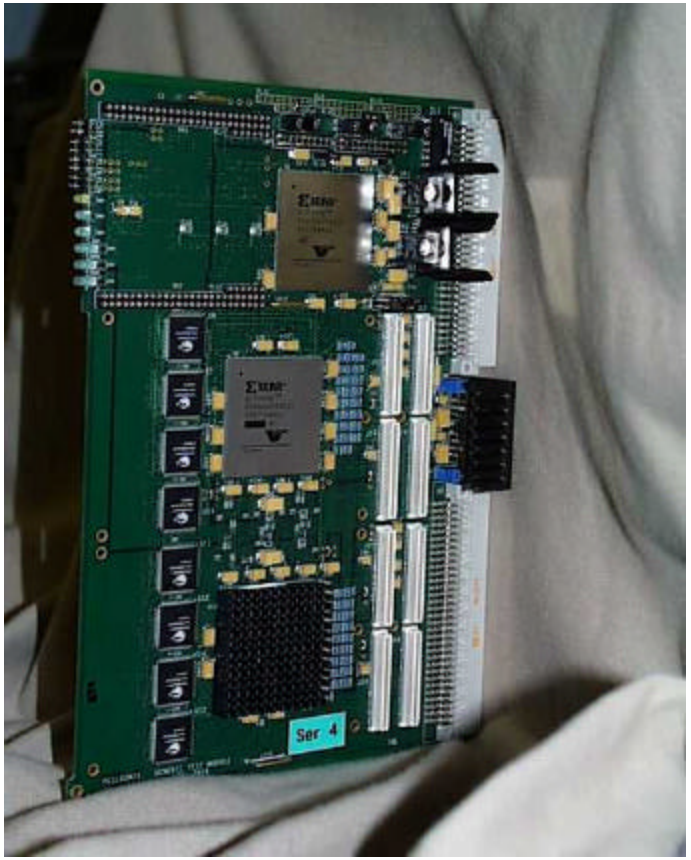
RAL

Test setup on GTM



- FPGA 1 (Two Configs)
  - Small set of vectors loaded into BlockRAM. (James)
  - Reads test vectors loaded into memory. (Ian)
- FPGA 2
  - CP chip

Initial Results - Calibration

- Eventually managed to get all 108 channels to successfully calibrate.
  - Debugged a number of “sillies”.
  - Required the 160 MHz serial to parallel converters to be “hand placed”.
- Warning
  - Other iterations may be temperamental.

Data Tests

- BlockRAM vectors
  - Quick visual check, some errors.
  - Steve thought that the errors were in the Right hand cells, the left seemed OK.
- DPR vectors
  - Some errors. Nothing obvious!
- Needs further investigation.

Xilinx Resources

- GTM (XCV1600E)
  - Number of Flip Flops:
    - 9,140 out of 31,104 29%
  - Total Number 4 i/p LUTs:
    - 21,480 out of 31,104 69%
  - Timing
    - 40 MHz (41.4 MHz)
    - 160 MHz (321.9 MHz)
- CPM (XCV1000E)
  - Number of Flip Flops:
    - 7,803 out of 24,576 31%
  - Total Number 4 i/p LUTs:
    - 18,305 out of 24,576 74%
  - Timing
    - 40 MHz (45.9 MHz)
    - 160 MHz (321.9 MHz)

Future Work

- Back in RODLAND!
  - Debug Slice AND RoI for Bruce.
- CP work partially suspended!
  - Debug Data transmission on GTM using ChipScope.
  - More simulations of Algorithm using Steve's test vectors.
- Other iterations of ROD when Spec arrives