LHC Clock Phase Stability: is it an issue?

- It seems that the LHC clock phase might drift relative to the beam crossing
- What can we tolerate, and will this be achievable?

Geneva, we have a problem…

Doesn't the TTC solve this for us?

- Not if it is the LHC clock itself which drifts relative to the beam phase.

Possible effects:

- Reduced FIR BCID efficiency
- Failure of saturated pulse BCID
- Degraded E_T resolution

Tolerances

From studies by PBT & Ullrich Pfeiffer:

- FIR BCID can tolerate ±5ns
  - BCID efficiency more sensitive than E_T resolution
- Leading-edge saturated pulse BCID fails at ±5ns
  - Probably strongest limit
- Both tested with em-like pulses
  - may be worse with hadronic?

Other sources of variation

We anticipated several sources:

- cable length variations
  - PPr can re-align phases
- time of flight variation
  - some p_T dependence cannot be corrected
- cell-to-cell timing differences within towers
  - cannot correct for these
  - specified to be $< \pm 2.5$ns

Drift vs Jitter?

What we can tolerate depends on period:

- "Jitter" (bc to bc variation):
  - effect depends of fraction of pulses outside tolerance (i.e. length of tails)
- Short-term drift (minutes to hours):
  - most dangerous: coherent effect on all events
- Long-term drift (days to months)
  - can recalibrate for this

So, what can we tolerate?

Assume other sources < 3 ns

- Jitter < ±2ns absolute (e.g. σ < 350 ps)

or

- drift < ±2ns on period less than recalibration

or

- appropriate mixture of the two

Limits depend on tolerable error rate

- assume rather low for saturated pulses

Effect on sLHC?

It's worse at 10^{35} $cm^{-2}s^{-1}$

- assumption is 12.5ns beam crossing interval
- will want to run 80 MHz BCID
- tolerance on phase variation will be reduced
  - approximately halved
- LHC clock drift tolerance may be very low indeed

So, where do we stand?

Nick is collecting requirements:

- I've given him the figures from slide 6

What can the machine do?

- No idea – anyone else?

Are others more sensitive?

- See above

Could we monitor phase?

Question from Nick:

- Can we monitor clock phase by analysing time frame data?
  - given enough data, I think so
  - best to use higher-E_T (non-saturated) pulses
  - monitoring jitter trickier

Conclusions

Not much tolerance left:

- Calorimeter readout uses up much of it

Don't know what LHC can provide:

- Best we can do is set an adequately tough requirement

We may be able to monitor drift:

- Needs some thought, but seems feasible in principle