19th March 2001

CP/JEP ROD Integration with ROIB and ROS

This test was possible only due to major effort by Bruce who wrote all the CPROD & DSS loading and checking software and also did most of the setting up and testing in Lab 8 and at CERN. Thanks also to Viraj and James for rapid responses to various problems.

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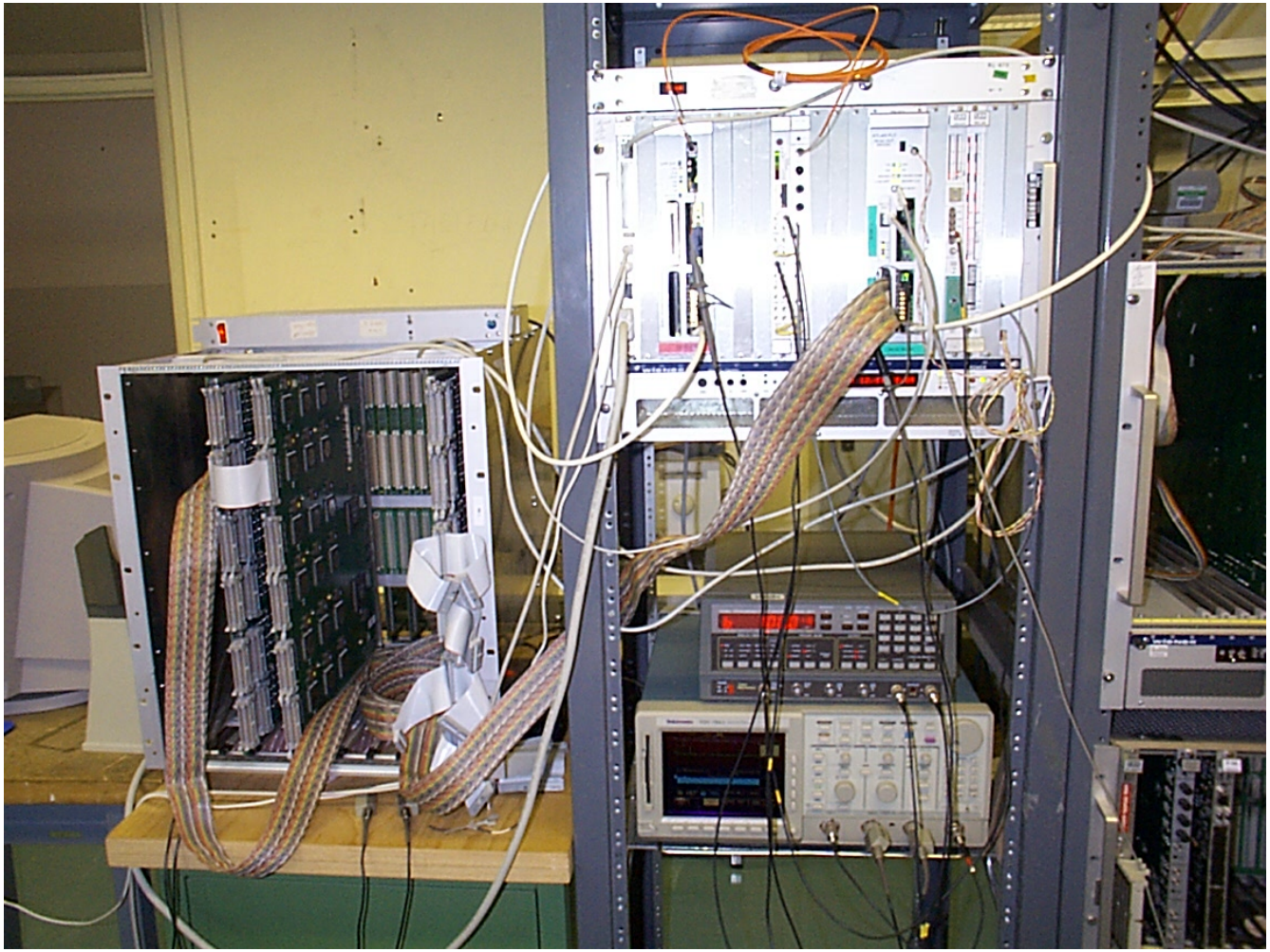
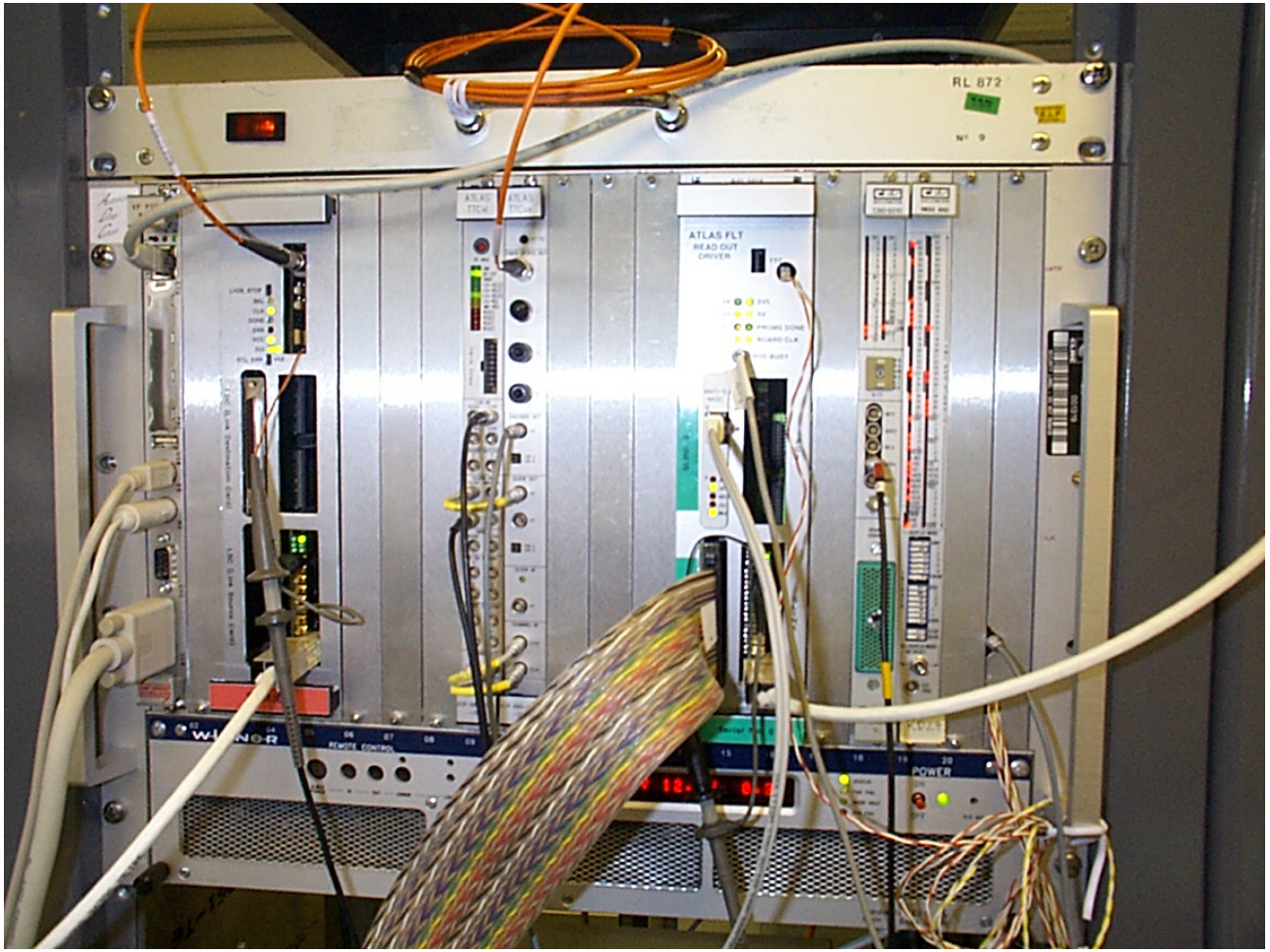
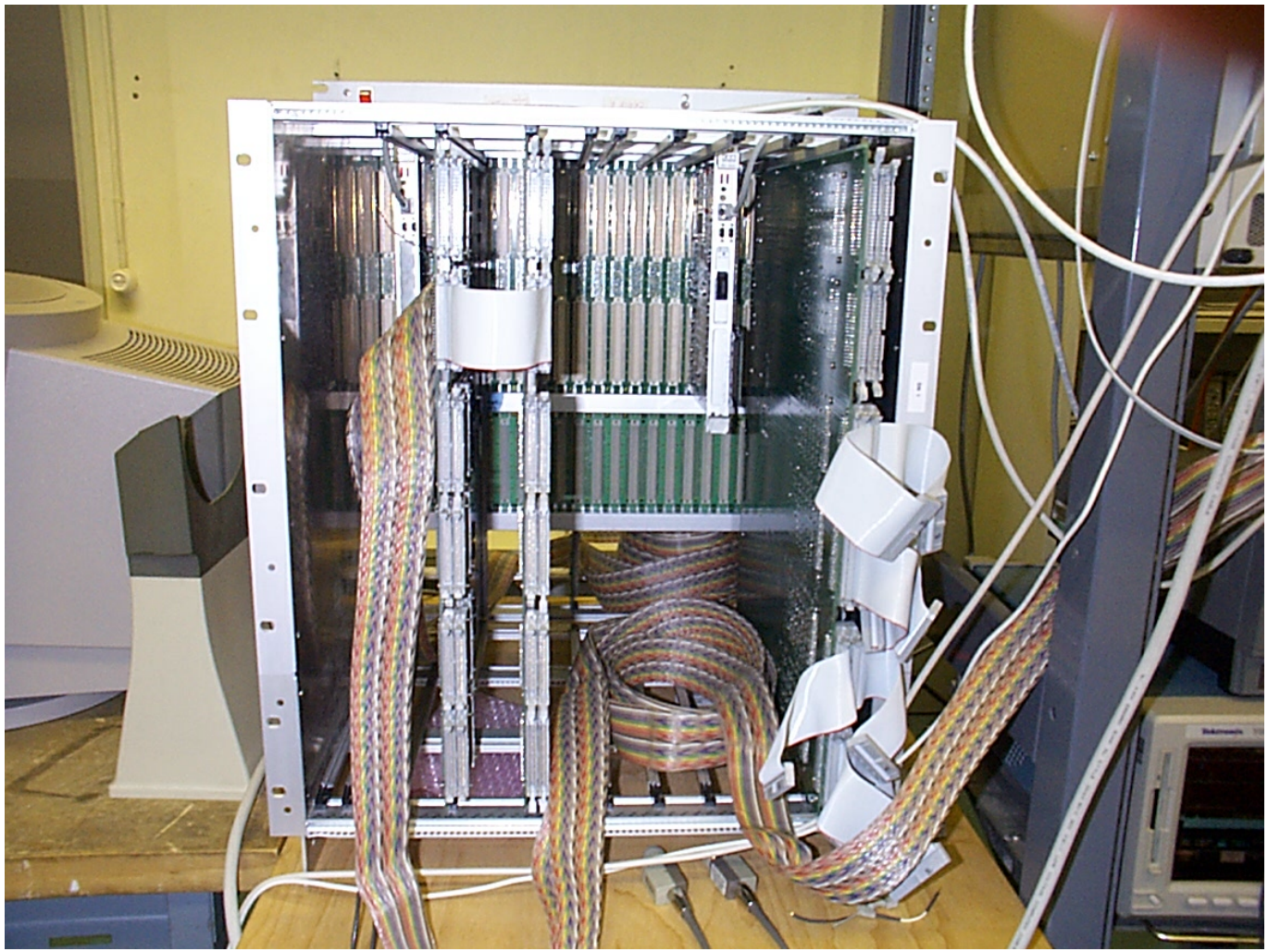
Overall Layout



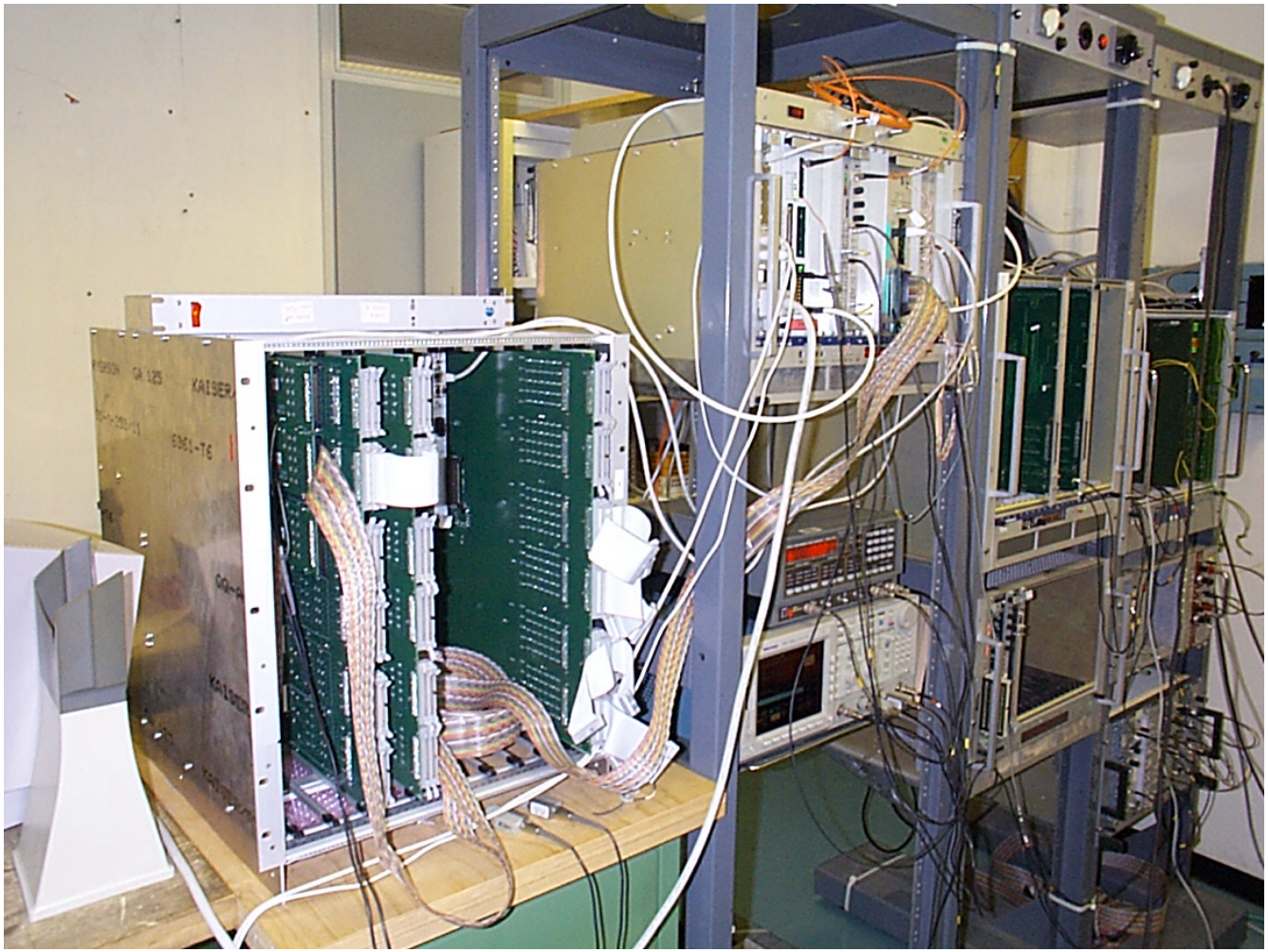
CPROD Crate



RoI Builder



RoIB, CPROD,CTP, & Muon systems



Muon Integration

Muon integration history:

- **Single event transfer - problems with 40MHz clock timing in RoIB (temporarily overcome for tests).**
- **Continuous transmission of same event:**
  - 40kHz L1A with checking of data received at RoIB
  - 100kHz L1A with no data checking except hardware control.
- **Latency measurement from L1A to RoIB.**

RoIB Input card timing modification:

- **MIROD now works with fixed 40 MHz timing to RoIB**

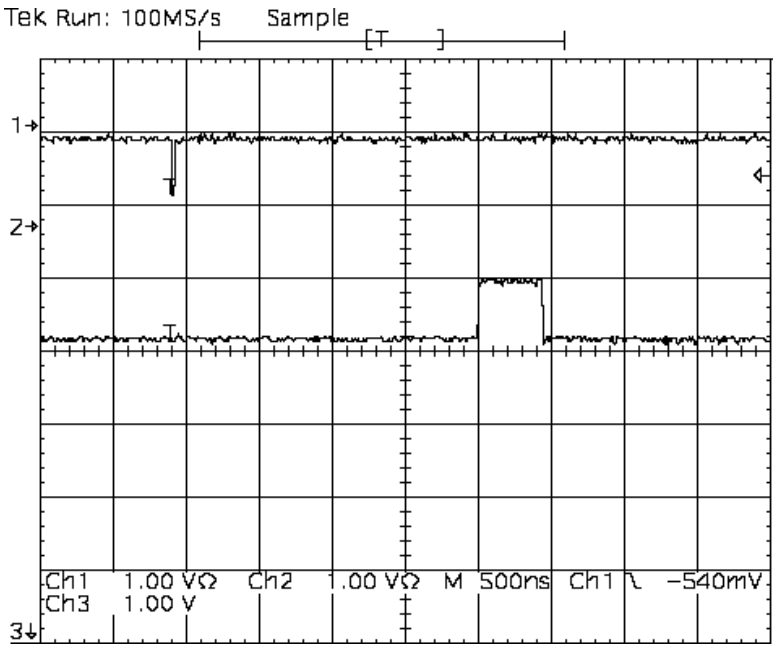
CPROD Integration Objectives

- Pass CPROD Self Tests to DSS [Yes]
- Transfer individual events to RoIB and check content [Yes]
- Run up to maximum speed limit (100 kHz) [No]
- Make a long run to check for low-level errors [Partial]
- Measure system latency L1A to readout. [Yes]
- Test with Full electrical S-Link to RoIB [No]
- Combined run with MIROD to RoIB [No]
- Run into ROS. [Yes]
- Combined ROS/RoIB Run [Yes]

Low Frequency Tests

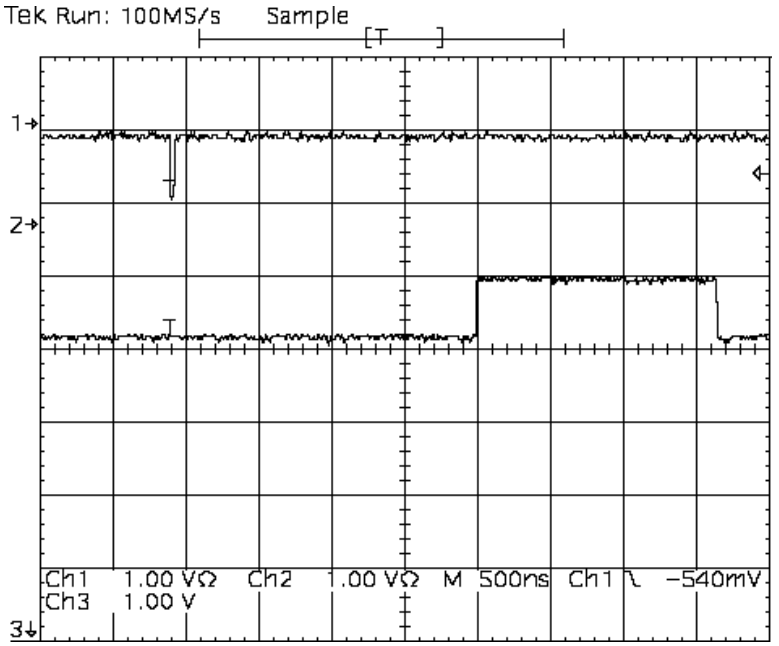
- **Test vectors provided by BMB in agreed format**
- **Improved Test program in RoIB (counts errors, ignores BC no and event no).**
  - Note: Errors not counted on long muon runs. As same event repeated, test not sensitive to missed events.
- **Data read and checked in parallel from second S-Link into DSS.**
- **Long overnight run: 16 RoIs, 31 longword (124 byte) events in bursts of 1024 events 2 mS apart, 3 S cycle, average 418 Hz, with full checking, 2.1 x 10^7 events without error. Corresponds to 2.1 x 10^{10} bits sent. This used ANL Pseudo S-Link.**
- **This was about the maximum rate sustainable without errors.**

Latency Measurements
Operation of ROD Busy



L1A

Busy



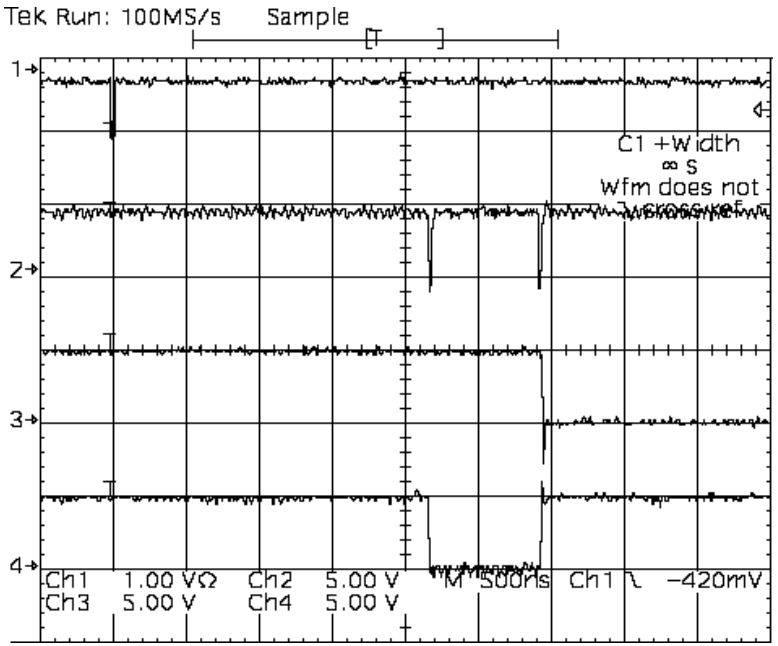
18: Busy, thr=3, 16 RoIs

i.e. 4 per FIFO

19: Busy, thr=3, 64 RoIs

i.e. 16 per FIFO

Latency Measurements - Time per event from L1A

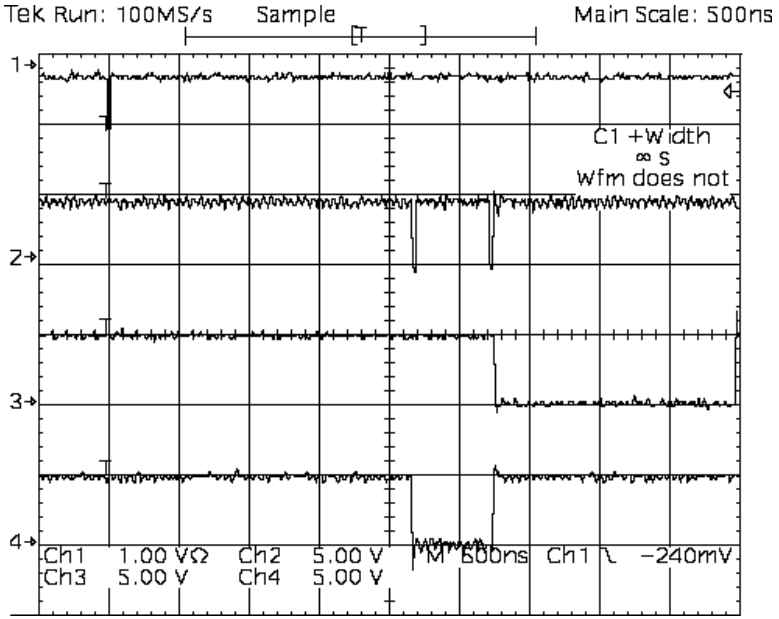


L1A

S-Link Control

LFF

Write Enable



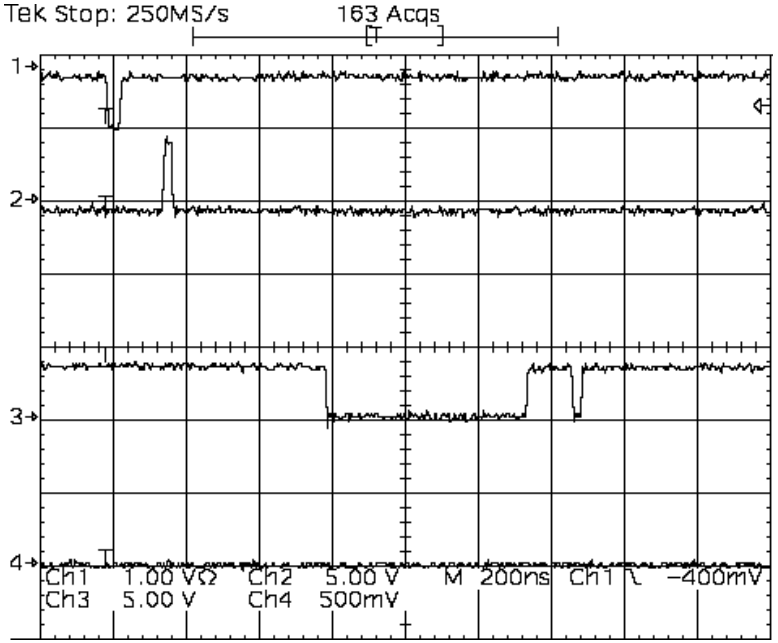
22: L1A to RoIB

31 longwords, 16 RoIs

23: L1A to end RoIB

23 longwords, 8 RoIs

Latency Measurements - Fine timing L1A to DAV

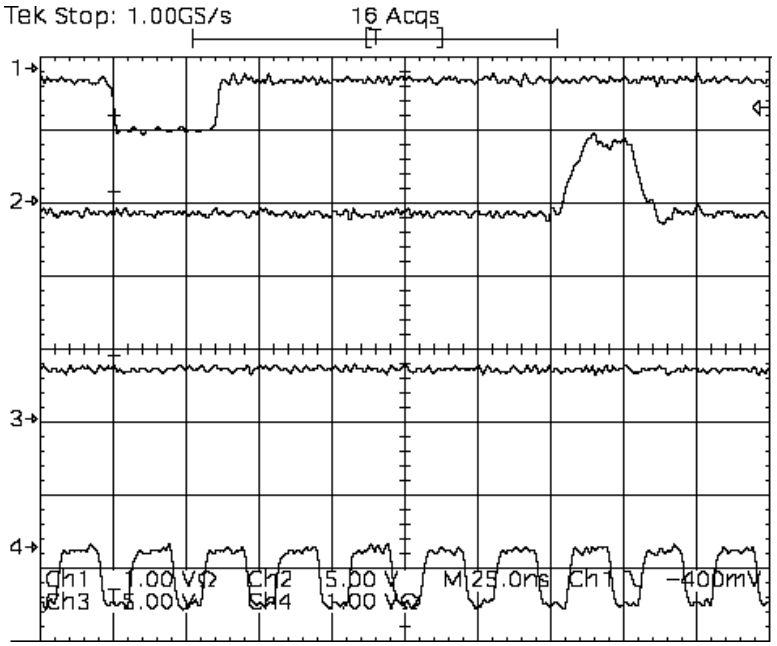


L1A to TTC

L1A from TTCrx

DAV

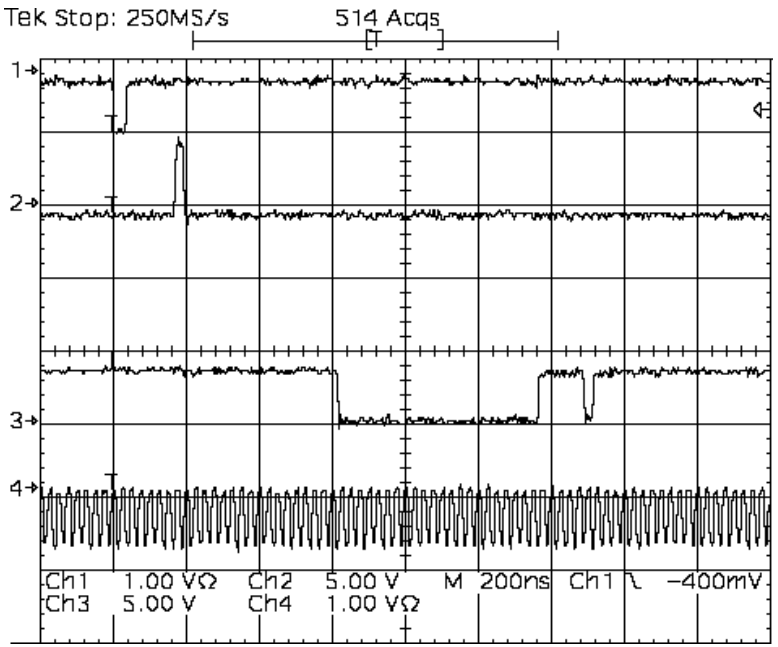
CLK 40



25:Timing L1A to DAV

27: L1A input & L1A at TTCrx

Latency Measurements - Strange G-LINK DAV behaviour

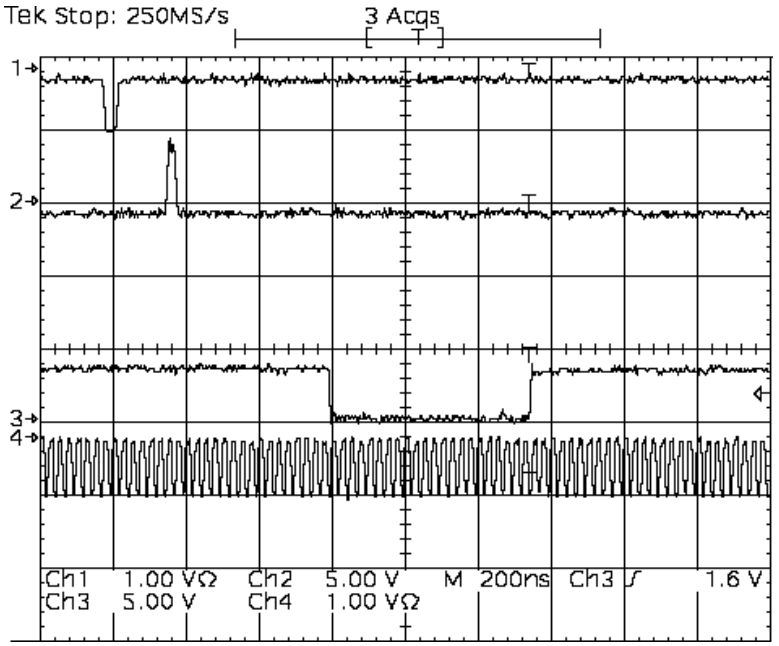


L1A

L1A at DSS

DAV at ROD

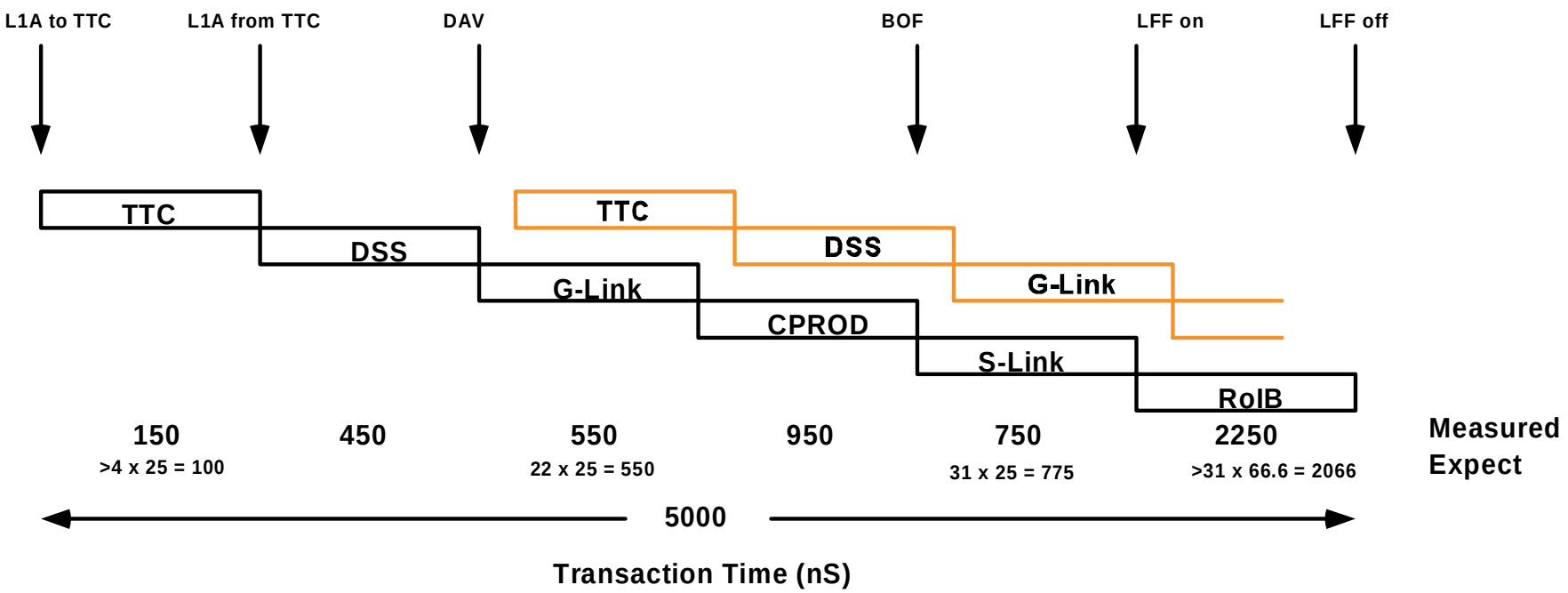
CLK 40.



28: Glitch in G-Link DAV

29: Another event, no glitch

Latency Summary



Flow Control - Slink protocol

- RoIB sets UXOFF# low when no more room for input data.
- Link Destination Card (LDC) transmits XOFF to Link Source Card (LSC)
- LSC stops data transmission.
- Last data packet from LSC travels via LDC to RoIB and is received there (may be tens of words after UXOFF# goes low)
- FIFO on LSC fills up, LSC asserts Link Full Flag (LFF#) when there is space for only 2 more words
- ROD detects LFF# and stops transmission within 2 words.
- When space available on RoIB, UXOFF# removed, LDC sends XON to LSC, LFF# removed, and ROD resumes transmission.

Flow Control - what actually happens

- At end of event, RoIB asserts UXOFF# and ignores any further data till the event has been moved to the main RoIB board.
- When CPROD receives LFF#, transmission continues for several more words. These are lost.
- When the RoIB resumes, it ignores data till a control word arrives. At high rate, this is probably an end-of-event marker. Eventually the RoIB or it's software becomes confused and hangs.

- New CPROD firmware handles flow control better, but occasionally loses or duplicates one or two RoI words, and the link memories containing the RoIs may not be emptied.

Tests with the ROS

- **Data transferred to ROS using the 2-fibre (i.e. slower) “ODIN” optical S-link:**
  - Various rates up to 20kHz with full data checking in ROD and
  - Instantaneous rates up to 666 kHz in bursts of 127 events
  - Check CPROD FIFOs to make sure the ROD doesn’t overflow.
- **Data transferred in parallel to ROS and RoIB using ODIN and APS links.**
  - Bursts of 127 events spaced 1 ms apart.
  - Several runs with an error appearing after around 2M events.
  - The same errors are seen in RoIB and ROS.

Miscellaneous lessons learnt

- There are still RoIB and CPROD firmware problems.
- It is hard to diagnose problems. Modules need test points and LEDs for key signals like L1A, LFF, DAV.
- We should buy S-Link diagnostic cards to exercise LFF etc.
- An undocumented value 22x can be set in CPROD status word 1.
- RoIB can hang if unexpected input is received. For all our modules, we should document the expected action if different types of unexpected input are received.
- One TTC input hole in a ROD front panel is in the wrong position!
- There's a strange glitch in the DAV signal.

Miscellaneous lessons learnt (2)

- The TTC assembly with interposer on one ROD is unreliable.
- The DSS power transistor cooling assembly is fragile and we need something better. The one I re-soldered needs checking.
- We are short of mounting pillars and screws for daughter boards.
- We should aim to have schematics for all modules and daughter boards accessible on the web, including a listing of the functions of the various test points.
- The silkscreen print on PCBs should identify connector pin 1.
- There is a tool by C. Schwick which documents VHDL into readable web pages.

Miscellaneous lessons learnt (3)

- It is possible to transfer FPGA designs to CERN and burn new EEPROMS, but the turnaround time is around 2 days. We must ensure that similar facilities are available in Heidelberg.
- Some ROD and DSS registers give BERR if the 40MHz clock is absent.
- The Concurrent can get into an endless loop when BERR is met, which is solved only by turning the crate off.
- It is very irritating having to stop and reboot the computer each time the crate needs to be powered down. Reboot is slow, is there some way to speed it up?

Miscellaneous lessons learnt (4)

- **The ROD can handle only 255 events at any time!**
- **Automatic wrapping of DSS (source) memory will be needed for future testing. You can't run at full speed without it, because the computer needs to intervene at the end of each cycle and this takes a long time.**
- **A 9U version of the RoIB is needed for September, running the DAQ-1 software. The timescale is demanding. We need to be involved in the review of the design.**

Some Conclusions

- **Lab in bat 595 is a bit small, but a good adjacent workshop, and we are grateful for the use of both.**
- **Georges Schuler and Ralf Spiwoks were very helpful, as were RoIB colleagues Jim Schlereth and Yuri Ermoline.**
- **We detected problems in CPROD and RoIB which needed to be found, particularly before the RoIB is rebuilt in 9U.**
- **The Muon hardware is not complete, and a re-test will be needed when the MICTP board is built. We need to think very carefully about how to run joint tests using the TTC.**
- **Well worth doing it.**