CPM Prototype

Project Specification, available at:

http://hepwww.rl.ac.uk/Atlas-L1/Modules/CPM/cpmspec103.pdf

Hardware Status

- CPLDs / FPGAs
  (other than Serialiser & CP FPGAs)
- Schematics
- Changes to PDR Document
  -> TTCrx access
- Timescales

R. Staley

THE UNIVERSITY
OF BIRMINGHAM

CPLD / FPGA status

Device	Implementation	Status	
VME interface CPLD	Altera 7000A series	VHDL ✓	☺
CPM Control FPGA	Altera 10K30E	Control / Status ✓ FLASH Configuration ✓ TTCrx Interface ✓ CAN Interface ✓	☺ ☺ ☺ ☺
ROC FPGA	Xilinx	ROC - Preliminary design in Altera AHDL Buffer Memory ✗ Hit Counting- Preliminary design in Altera AHDL	😐 ☹ 😐

Schematic Status:

A framework of 16 sheets exists:

1	VME Address decoder + address bus	
2	VME Data Bus + Module Control	
3	TTC + clock distribution	
4	CAN Controller	
5	ROC + HIT logic	
6	LVDS Rx + Serialiser	X 10
7	CP Chips	X 8
8	Module Power Supplies	
9	JTAG chains	
10	LEDs	
11	Backplane connectors 1/2	
12	Backplane connectors 2/2	
13	Serialiser Configuration access	
14	CP chip Configuration access	
15	Serialiser Power connections	X 4
16	CP Chip Power connections	X 2

Estimated total number of A2 sheets ⇨ 36

Changes to PDR Document -> TTCrx

Power-up Address Settiing

6 LSBs of 14 bit chip ID → I2C base address

- If the TTC I2C address is to remain fixed (desirable) then Modules of a particular type will not have sequential TTC ID values.

Access from VME

Read / write operations to the TTCrx are performed over the I2C serial bus. The I2C interface is a simple register and the protocol managed by software.

- The TTCrx registers will NOT be mapped into a VME address space. (Unnecessary hardware complications.)

Timescales

	Dates
Schematic Design finish	mid. Feb. 2001
Layout finish	early April 2001
Manuf. + Assembly	early May 2001
Module test (B'ham)	June 2001
CP system test	July 2001
Available for Slice Test	Aug. 2001

Additional comments arising from presentation.
(as of 26/1/2001)

1. A ☺ = VHDL > 90% done . Device pin-out can be assigned.

   A 😐 = AHDL work to be transferred to VHDL

   A ☹ = VHDL to be taken from Serialiser design and modified

2. Schematics are now on 18 sheets, with FLASH configuration circuitry and ROC + Glinks now moved to additional pages.

   The 'x N' in the second column means the structure of the schematic drawing will be copied onto N Sheets.

3. Timescales for Module testing have been compressed to be complete for Aug. 2001. A longer period is desirable.