Design Reviews

1. PDR for Common Merger Module (CMM)

- **Draft 3 of the specifications written by Norman**
- **Review Panel:**

  Eric Eisenhandler

  Uli Schaeffer

  Sam Silverstein

  Richard Staley

  — supplied written comments in advance

- **Additional comments from Ian, Murrough and Viraj**
- **PDR held at RAL on Monday 11th December 2000**
- **Reviewers comments addressed by Norman in comprehensive written response**
- **Many minor *(and some not so minor)* amendments and clarifications to both text and figures discussed and agreed**
- **No unresolved disagreements about any significant points**

- **Several general areas which had been noted by the reviewers were discussed during the review:**
  - **VME access contention *(system-wide)***
  - **Interface to CTP — signal levels and timing**
  - **G-link data packing scheme**
  - **Event data overflow handling**
  - **On-board clock distribution**
  - **Overall latency estimates**
- **Overall conclusions from the Review:**
  - ***The CMM has evolved into a well-specified generic design***
  - ***It provides efficient re-configuration for system or crate merging functions for a wide variety of triggers***
  - ***The schedule is very tight, and on the critical path for Slice Tests***

- ***Some of the more important points raised:***

- **DEFINE — Main jet trigger *(not non-forward or central)***

- **DEFINE — Crate/Module numbering scheme:**

  CP System — Crates 0-3, CPMs 1-14

  JEP System — Crates 4-5, JEMs 0-15

  (PPr System — Crates 0-15, PPMs 0-15)

- **Module type — CMM = 2417 in RAL register**

- **Module serial no. to be defined by solder jumpers**

- **Data readout format to be identical for System and Crate CMMs → uniform ROD firmware**
  (C-CMM sets System data to zero)

- **ALL cable I/O signals will be LVDS *(no ECL)* — define cable specifications and grounding details *(must agree with Processor Backplane scheme)***

- **Backplane cable connectors to be 64-pin IDCs**

- **Specifications of cable input daughter-cards to be defined in Appendix 1 *(Backplane pin-list)***

- **Backplane signals to be defined as single-ended back-terminated 2.5V CMOS**

- **Confirm CTP *(and CTPD)* input signal specification — including timing requirements**

- **LVDS-PECL converter required to feed CTPD in Slice Tests**
- **Single ISP port per CMM — internally chained to all FPGAs**
- **TTC Broadcast must allow simultaneous playback across all CMMs**
- **Separate PULSE Control Register to be provided**
- **L1ID will not be included in the readout bits *(complication for ROD at this late stage)***
- **Specify skew on incoming CPM HIT bits to be = 10 nsec**
- **All = 40 MHz signals to be routed on controlled-impedance traces of defined value**
- **Only +5V supply will be used — other supplies derived from on-board regulators as required**
- **Presence of ALL external and internal power supplies to be indicated by front-panel LEDs**
- **Add conceptual module floor-plan to indicate inter-chip routing**
- **Latency to be defined within the overall calorimeter trigger latency envelope**
- **Revised schedule — FDR 04/01, Testing 07/01**

2. PDR for Jet/Energy Processor Module (JEM)

- **Draft 0.1 of the specifications written by Carsten, Uli and Sam**
- **Review Panel:**

  Norman Gee

  Murrough Landon

  Paul Hanke

  Richard Staley

  — supplied written comments in advance
- **Additional comments from Eric**
- **PDR held at RAL on Tuesday 12th December 2000**
- **Many minor *(and some not so minor)* amendments and clarifications to both text and figures discussed and agreed**

- **Several general areas which had been noted by the reviewers were discussed during the review:**
  - **Supply voltages — generation, distribution and allocation**
  - **Grounding scheme**
  - **Clock distribution**
  - **TTCrx provision**
  - **Alternative input data synchronisation scheme**
  - **Latency breakdown — estimates**
  - **Board dimensions — depth, no. of layers, thickness constraints**
  - **Status of schematics and layout — schedule**
- **Overall conclusions from the Review:**
  - ***JEM specifications document now very comprehensive***
  - ***Design framework generally appears sound***
  - ***Concerns that in some areas it may not conform fully to Module-0 requirements → Slice Test System integration problems?***
  - ***Aggressive schedule prevents any significant hardware design changes***

- ***A few of the more important observations:***

- **JEM refers to the Jet/Energy module**

- **Differences in specification between this design and Module-0 must be clearly identified**
  (e.g. in Appendix)

- **External 3.3V supply *should* be used only for LVDS de-serialisers to ensure cleanliness**
  — but also feeds CPLDs, Flash memories and LVDS-related CMOS

- **Synchronisation of the input data from the LVDS de-serialisers will use the IB scheme *(as in CPM)* unless input-FPGA resources prove too limited**
  (US's alternative scheme needs PPMs to play back timing calibration data after every power-up)

- **The RoI definition for jets should be identical to the one used for the CP system, and described with the aid of a diagram**

- **Many changes suggested to the Programming Model *(adding registers, re-arranging bit fields, …)***

- **A latency breakdown estimate should be provided**

- **CAN controller will be CERN-supported ELMB card *— in contrast to PPr and CP systems which will use the Fujitsu micro-controller***

- **The grounding scheme should conform to the PPr/CP proposal, following the PB review**

- **Concern about overall board thickness — if controlled-Z traces increase it to 2.5mm, only 1.5mm clearance for components on back face**

- **Was proposed to reduce board depth to 300mm with extension section *(cost-saving measure)* but it was very strongly recommended that the standard 400mm depth be used**

- **Schematics and layout almost complete — board manufacture in January**

- **Conclusions:**

  - **Although there are several areas which would benefit from more discussion, there are no obvious "show-stoppers"**

  - **The module should work *— and hopefully should be fully-compatible with all other hardware and software in the Slice Tests***

3. PDR for PreProcessor Module (PPM) and PreProcessor ROD (PPROD)

- **Agreed at November Heidelberg Joint Meeting to review these 2 designs together in the same PDR**
- ***Very preliminary* draft specifications of PPM were already then available**
  — status of PPROD specifications unknown
- **PPM hardware description was essentially ready — programming model currently being completed**
- **Final specifications available by February 2001**
  — lack of people has delayed overall schedule by 2-3 months
- **PDR currently expected to be held in Heidelberg during February 2001**
- **Proposed Review Panel:**

  Bruce Barnett

  Steve Hillier

  Gilles Mahout

  Uli Schaefer

4. Schematics Review for CPM

- **Schematic capture almost complete**
- **Aim to finish by February 2001**
- ***Informal* review during February *(Viraj + 1)***

5. FDR for PreProcessor MCM

- **Final details delayed until PPrASIC footprint established**
- **Aim to complete all documentation by March 2001**
- **FDR proposed for March 2001**
- **Original (PDR) Review Panel:**

  Christian Bohm

  Paul Bright-Thomas

  Viraj Perera

  Uli Schaefer

- **Some changes obviously necessary!**
  — proposed FDR reviewers:

  Gilles Mahout

  Viraj Perera

  Uli Schaefer

  A N Other (ATLAS Tech. Co-ord. nominee)

6. PRR for PreProcessor ASIC

- **"Low-key" PRR had already been agreed with ATLAS Tech. Co-ord. *(Erik van der Bij)* :**
  - **confirmation that all FDR recommendations had been followed**
  - **check-list completed**
  - **documentation fully updated**
- **Unfortunately, loss of key Heidelberg people has led to revised plan *(now approved by Nick Ellis)* :**
  - **engineering run of 3 wafers April-May 2001 → *sufficient dies for MCMs for Slice Tests***
  - **wafer probe testing June-July 2001 before assembly on to MCMs**
  - **PRR *(including results from tested MCMs)* in September 2001**
- **Full production run of ASICs will follow Slice Tests**