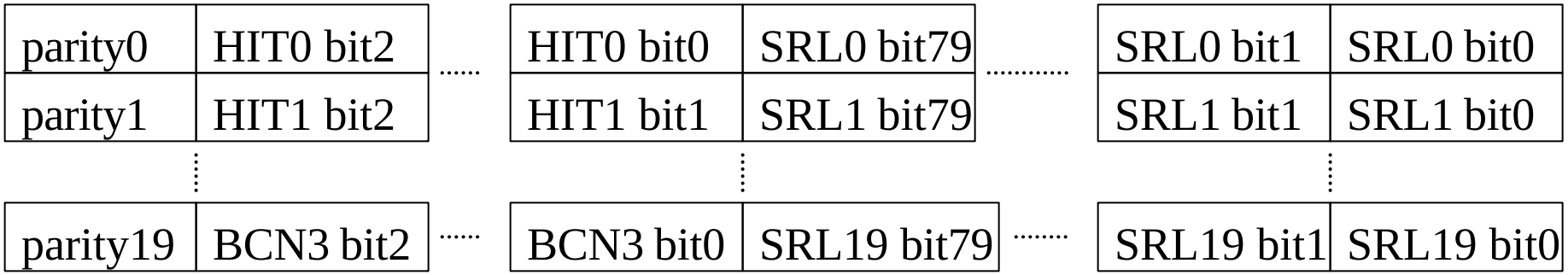
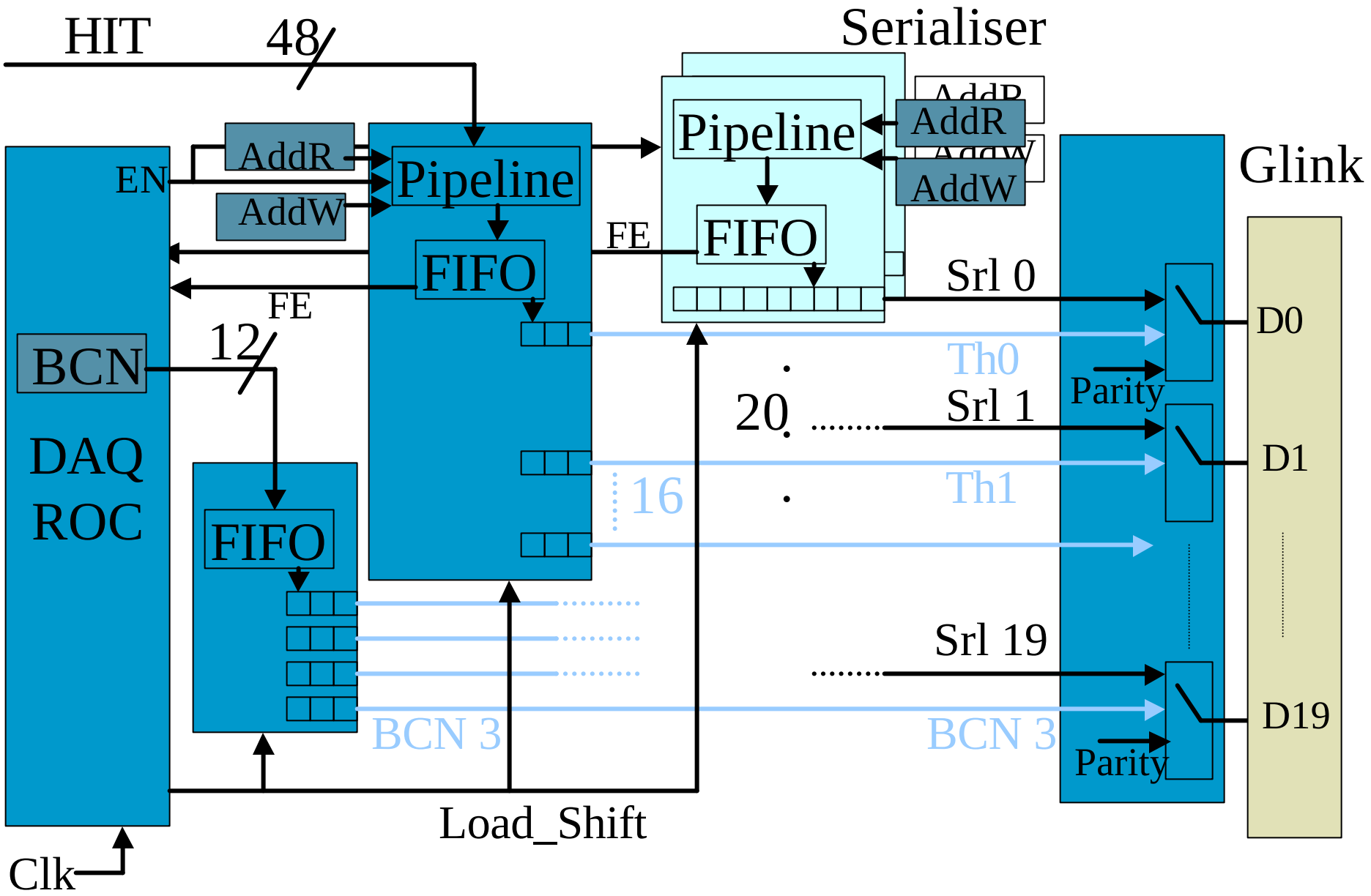
CPM Readout Controller Design

ROC functionalities: DATA path to ROD

- On LVL1A receipt, Enable Readout (EN): output data contained in DP memory at address ADDW+ offset in FIFO
- If FifoEmpty (FE) not empty starts LoadShift
- Enable shift register of data from the serialiser …
- …then Hit results, Bunch Crossing Number and parity bit



ROC functionalities



ROC: VHDL design

- Thanks to Ian and Richard, several blocks were available:
  - Pipeline (same as serialiser chip)
  - Fifo
  - Counter
  - Multiplexing
  - VME controller
- Functional tests are OK
- Implementation in Xilinx Virtex XCV100-6-pq240: 98 % bonded IOBs: more pins could be saved
- Simulation with timing: does not work: suspect timing problem between Fifo output and shift register

Next Step

- Find timing problems
- Testing VME control
- Design the RoI ROC: 16 pins output of 21 bits each