LVDS Transmitter and Receiver Cards for the DSS

- **CMC I/O Card**
  - 33 differential I/O pairs (32 data + one clock) or 66 single ended
  - Based on Xilinx Virtex-E FPGA (XCV300E-BGA432)
    - This allows the card to be a transmitter or receiver
    - Can generate other I/O standards (LVCMOS, PECL, BLVDS, etc)
    - Benefits using FPGA
      - One PCB design for different I/O standards, receivers and transmitters
      - Can load fixed test patterns from the FPGA on the CMC card instead of the DSS if required.
      - Can introduce delays in different paths to test synchronisation issues
      - Implement PCI interface with a PCI core
  - 3 x CMC connections (J1 to J3) as per DSS specification
  - J4 CMC as per GTM specification
  - JTAG access to program the EEPROMs in-system + access to the FPGA

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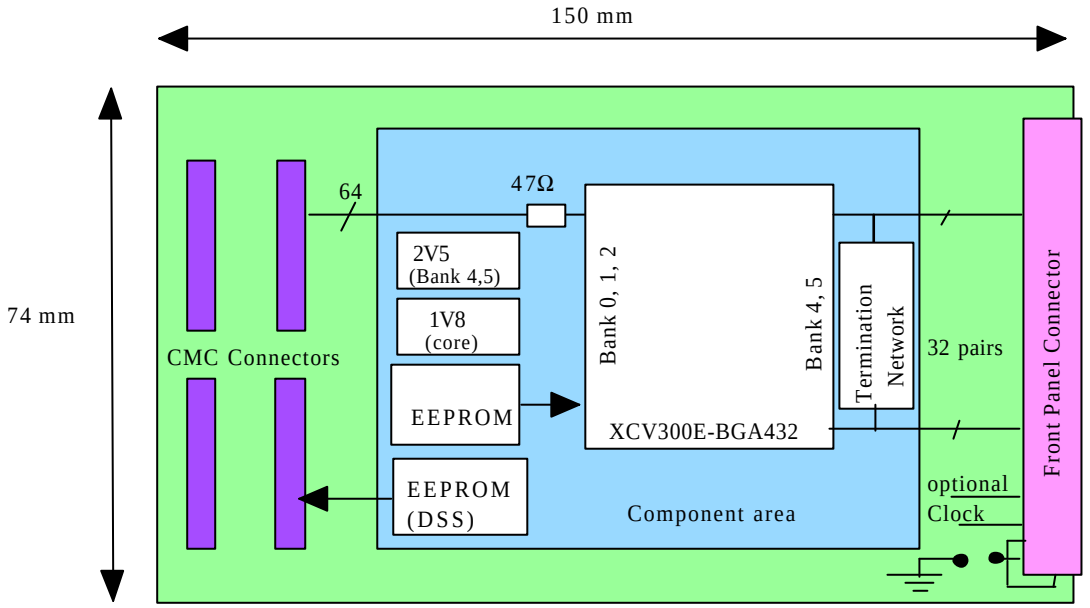

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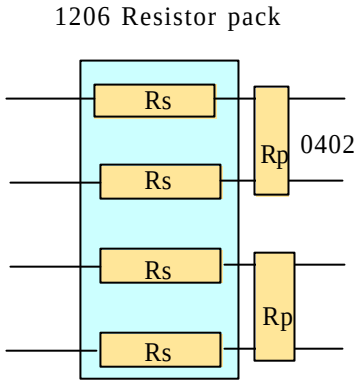
- Assemble appropriate network depending on transmitter/receiver or CMOS, LVDS, PECL etc.

I/O Type	**Rs** W	**Rp** W
LVDS Receiver	0	100
LVDS Transmitter	165	140
BLVDS	47	100
Single ended CMOS, LVTTL	47	open
PECL Receiver	0	100
PECL Transmitter	100	187



- Specification at http://www.te.rl.ac.uk/esdg/atlas-flt/ under DSS daughtercards

LVDS Transmitter and Receiver Cards for the DSS

- Type of connector to use
  - 68 way SCSI-3 connector is suggested, however some concerns from CERN regarding reliability.
    - Fits nicely on a CMC format
    - Latched connectors
    - Round cables with screen
    - Same type for CMM to CTP connection (2 connectors on the front panel)
    - CMM Rear Transition Module (three connectors)