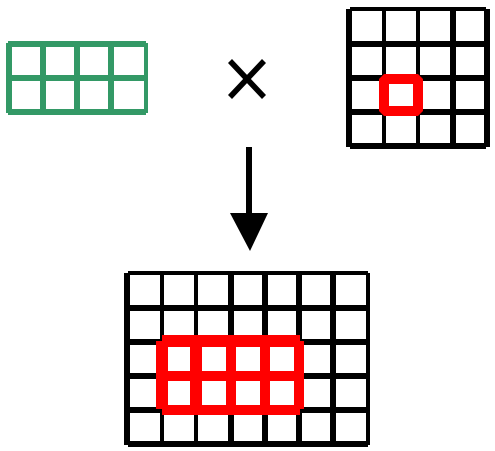
CP Algorithm Placement – ignore the bottom or top row?

- How did the problem arise?
  - Reminder of CP Environment
  - BC-Multiplexing Considerations
- What are the advantages/disadvantages
- Illustration of PPM to CPM/JEM mapping
- Note on physical modules

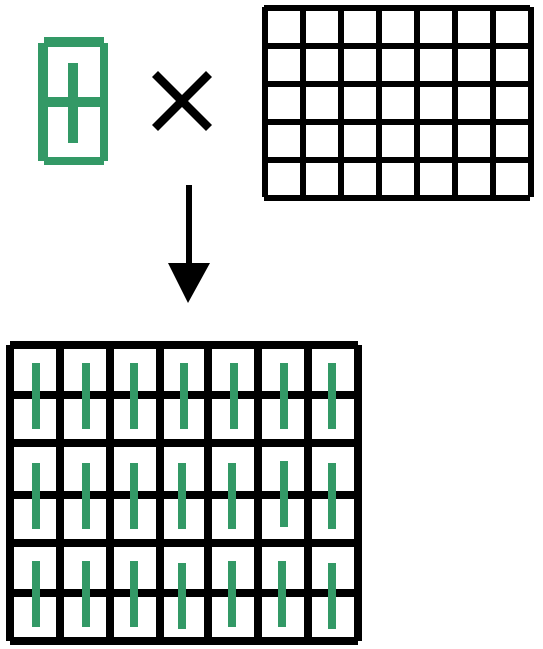
CP FPGA Environment

- CP FPGA processes 2x4 reference cells
- Algorithm requires 4x4 cells around reference
- Convoluting these gives 5x7 FPGA environment

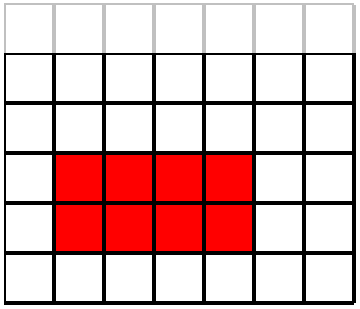


BC Multiplexing Considerations

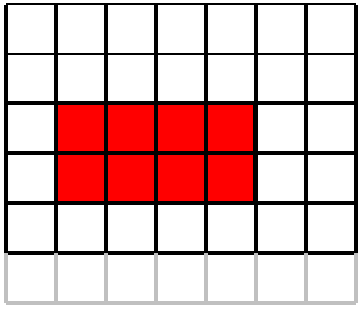
- BC-MUX ties together two towers in phi (2x1)
- Already have 5x7
- Convoluting these means that CP FPGA receives 6x7 cells
  - As 21 BC-MUXed pairs (per layer)



The Problem – Two choices



- Discard the top row
- Bottom-left cell = (1,1)
- CP Chip Specification

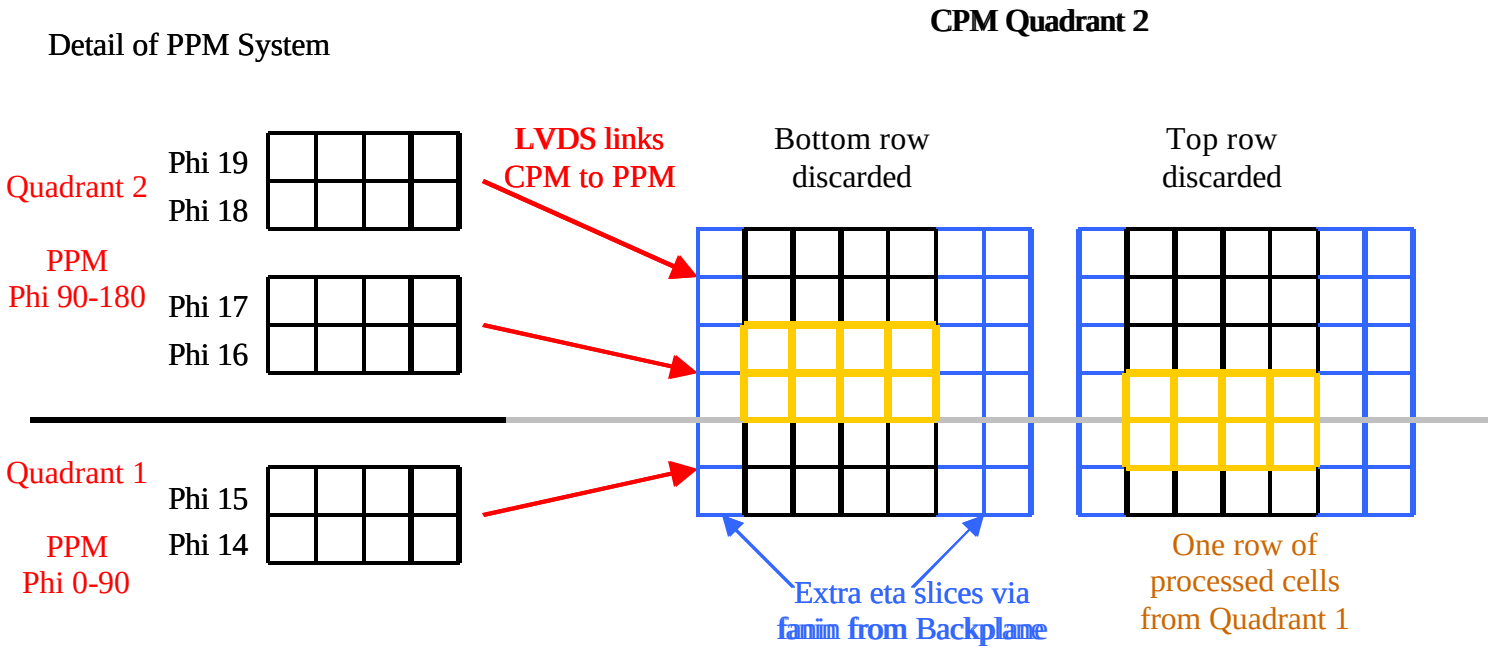


- Discard the bottom row
- Bottom-left cell = (2,1)
- CPM Specification

Pros and Cons…

- CP FPGA Specification
  - Obvious choice for CP chip in isolation
  - The code already exists!
- CPM Specification
  - Conforms to architecture decisions in TDR etc
  - Chosen to simplify PPM to CPM cell mapping
    - Reference cells processed by one CPM map directly from one EM PPM and one Hadronic PPM
- NB: Both do the job if applied consistently

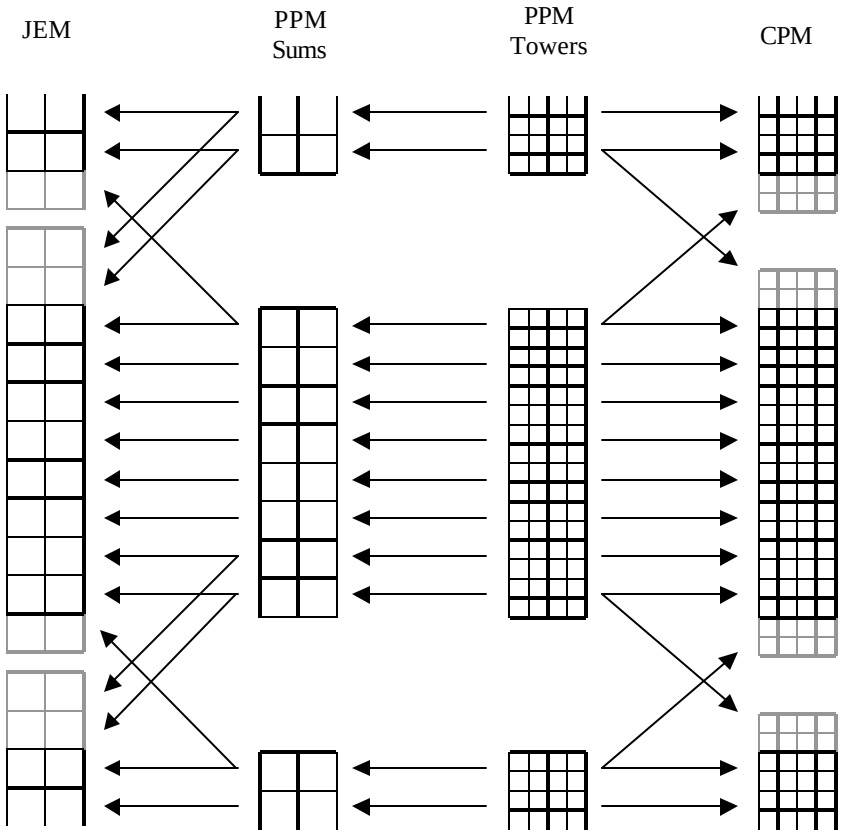
Detail of PPM to CPM edge mapping



Thoughts

- System can be built either way
- Potential for confusion greater with current FPGA code
- System is already complex, don’t want to make it more so
- See supplementary notes on cabling fun

Illustration of phi mapping in PPM to CPM and JEM systems



Physical PPM to CPM/JEM mapping

- PPM has low phi at top of module
- CPM has low phi at bottom of module
- JEM (as far as I can tell) has no preference
- Whatever happens there is likely to be some cable spaghetti