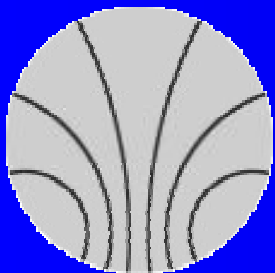# Testing the PPrASIC

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KIP, University of Heidelberg

ATLAS Level-1 Calorimeter Trigger Collaboration Meeting

Birmingham, November 7th, 2002

# Overview

- Reminder (Stockholm Meeting)

- Hardware Setup

- LVDS Synchronization Pattern

- Analog Input to the MCM

- Real-time LVDS Output to

  – Jet Processor

  – Cluster Processor

- Summary and Interpretation

- Outlook

# Reminder: Stockholm

- No analog inputs to ADCs
- No configuration access: relied on hardware default settings
- No Readout
- Power-Up Tests
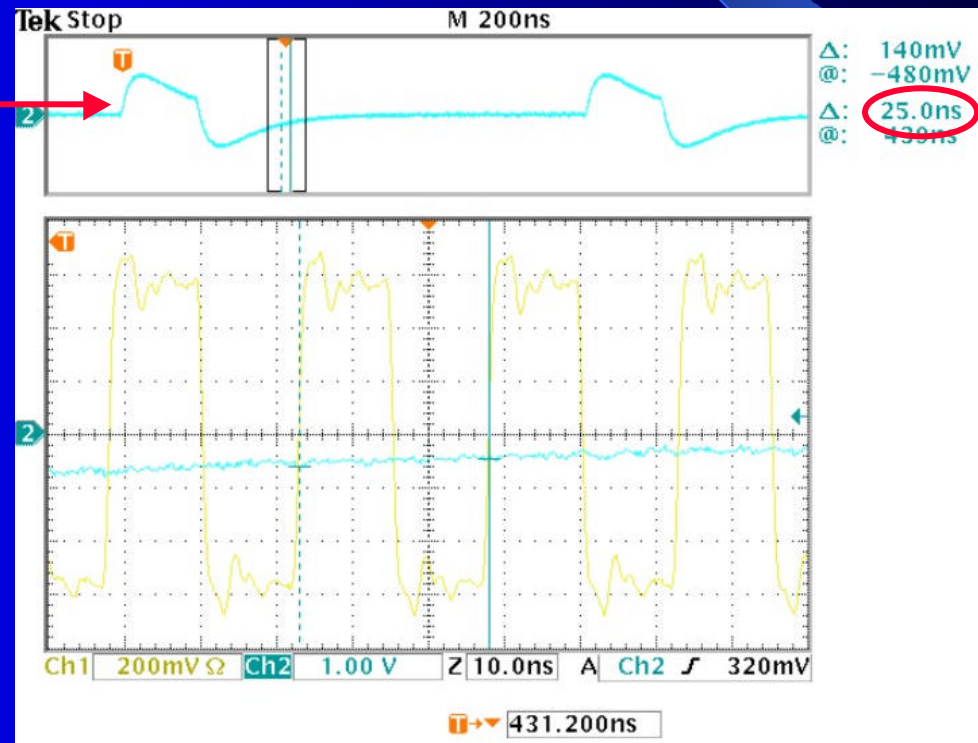- System clock with 40 MHz generated onboard
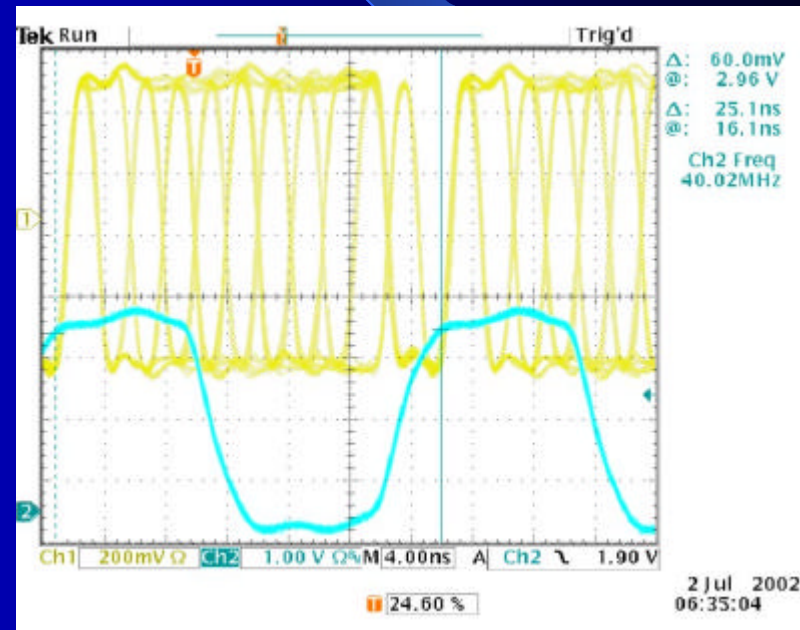
# Test Setup

- Testboard with MCM and AnIn
- Oscilloscope with differential probe
- Analog input generated by resonant circuit (L=4.7μH, C=820pF)
- Still no connection to crate for readout
- No video signals yet
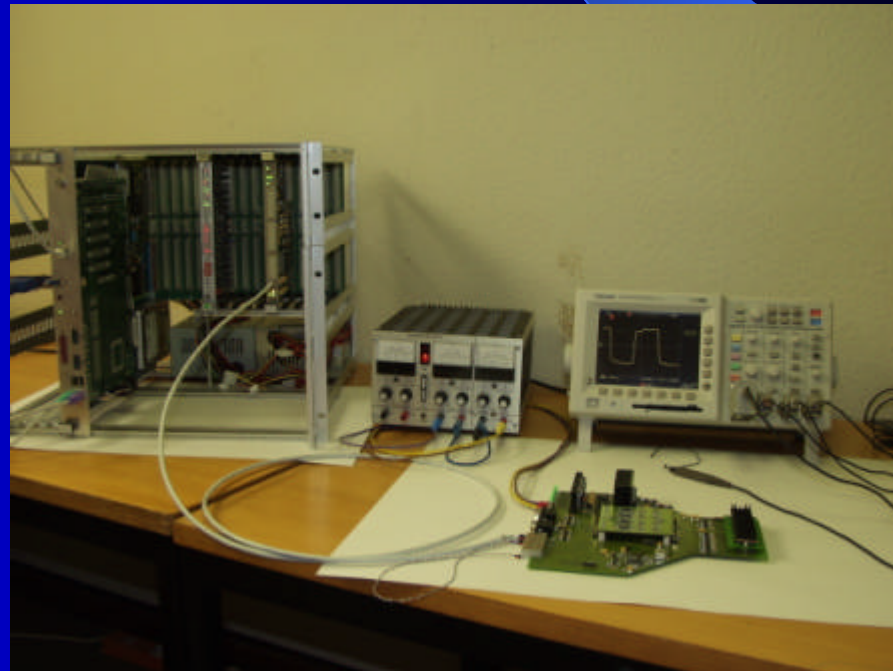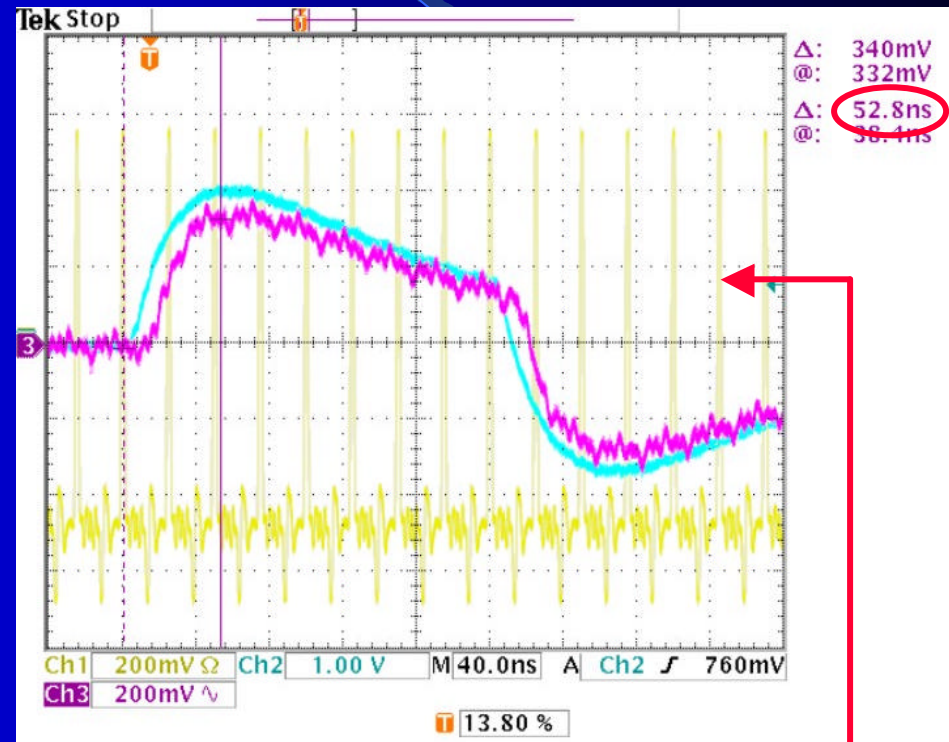
# LVDS Synchronization

Successfully initiated LVDS Sync pattern from MCM senders
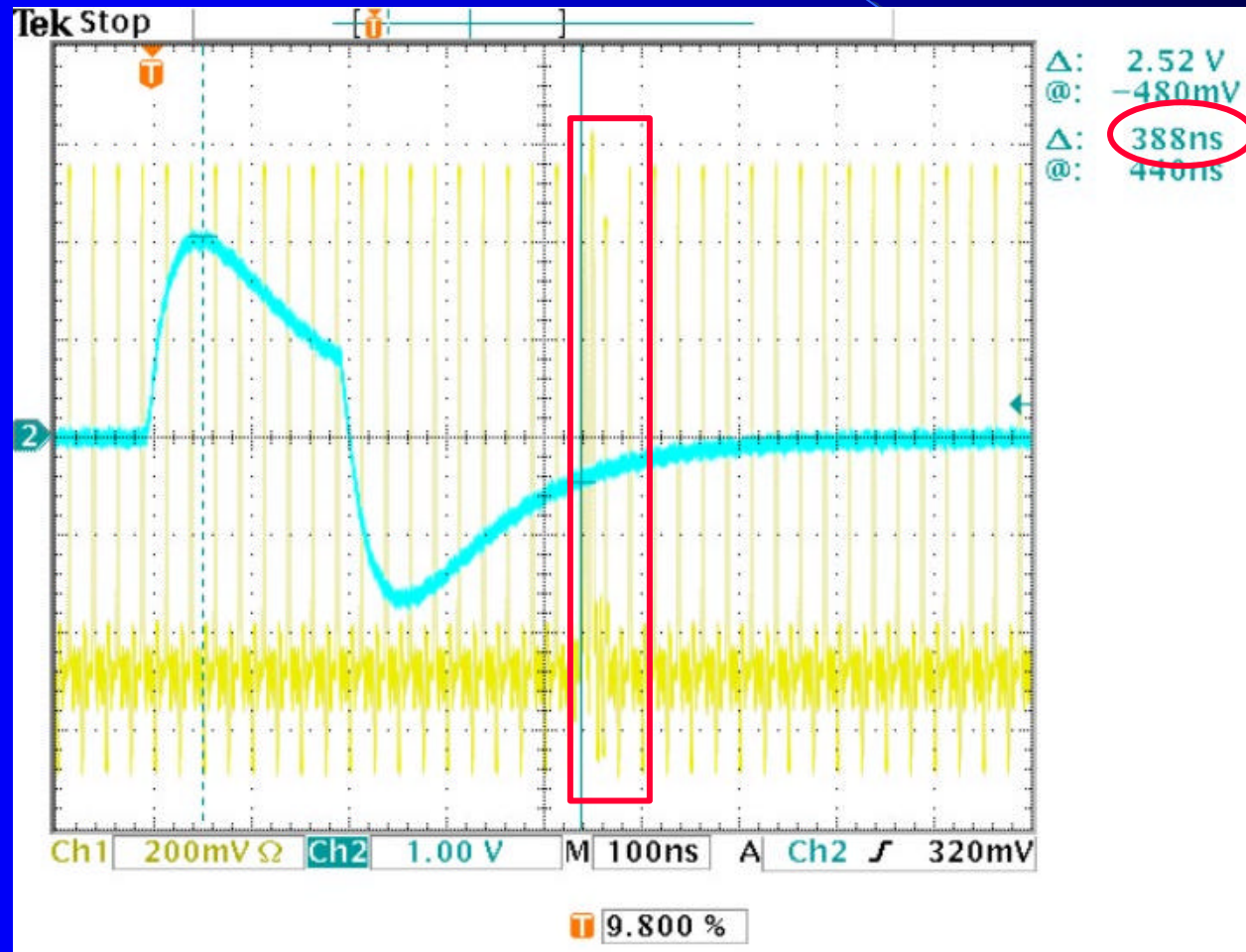
Analog Input

# Analog Input Signal

- Amplitude: 2.15 V
  FADC input window:
  1.9-2.9 V $\Rightarrow$ 250mV
  above threshold

- Rise time: 50 ns

- Delay through
  AnIn: 8 ns

- LVDS output
  constantly zero
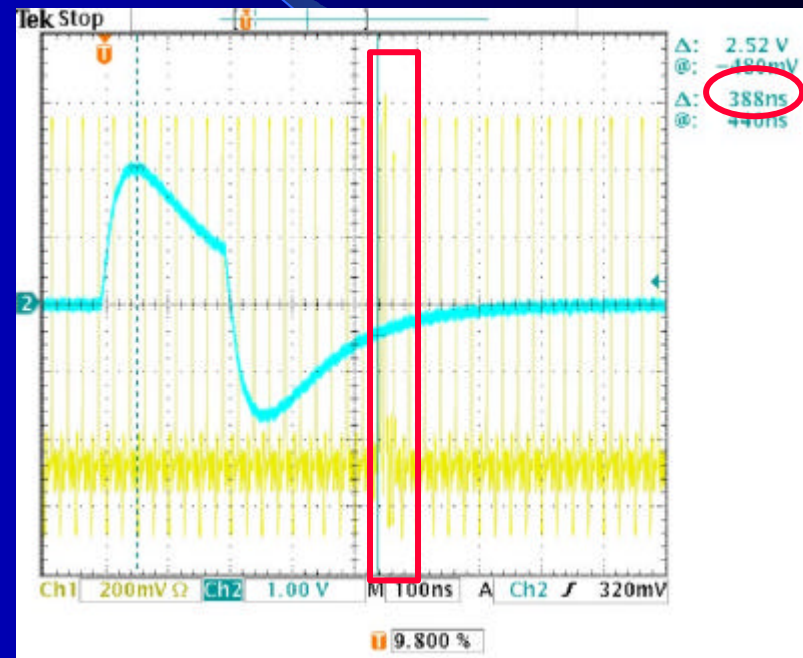  within the displayed
  time window:
  Wrong Parity!

# LVDS Response (Jet/Energy)

# LVDS Response (Jet/Energy)

- Time difference between signal peak and response: 388 ns (16 bunch-crossings)
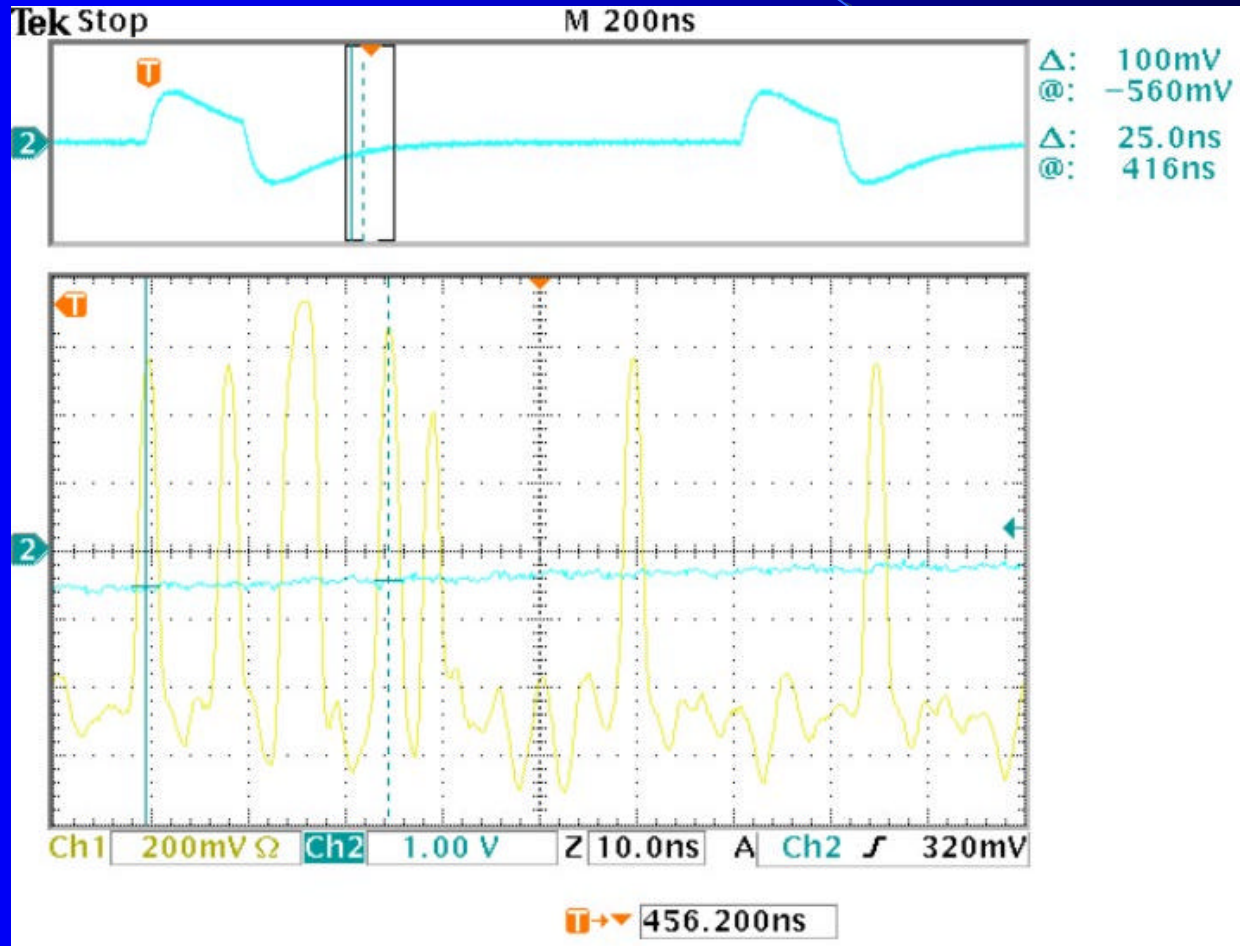- Zero data are transmitted during all other time frames

# LVDS Response (Jet/Energy)

- Data pattern remains absolutely stable
- Non-zero data are only issued in a single time frame
- MCM is sensitive to minor changes of the input signal (2 LSBs)
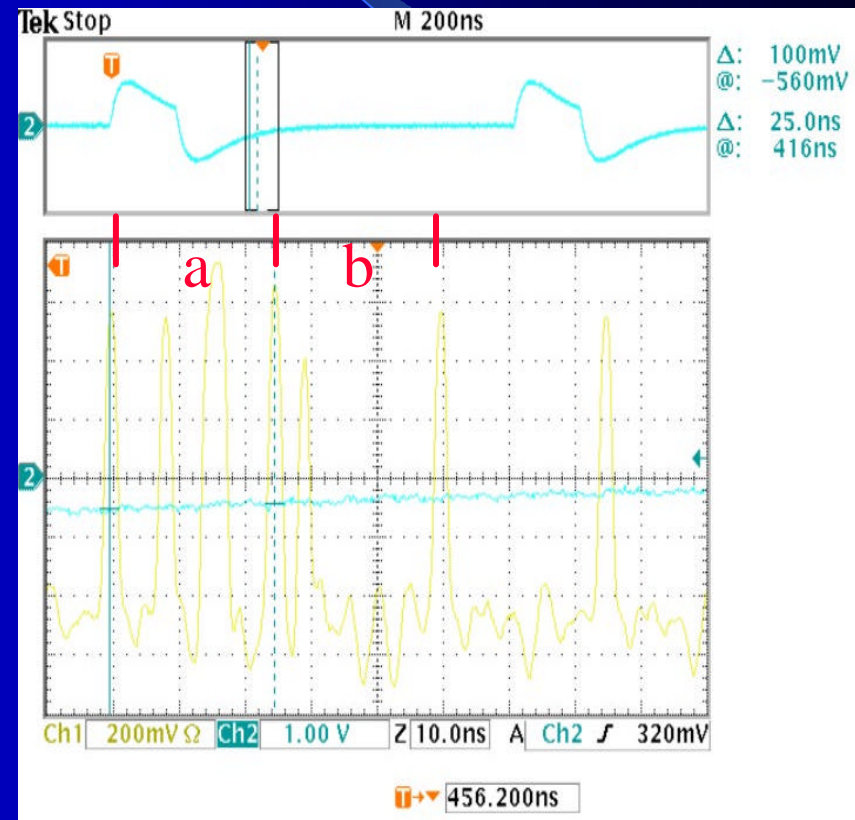- Observed pattern: 0100_1100_00 (dec: 50) expected: 250 mV/4 = 63 mV
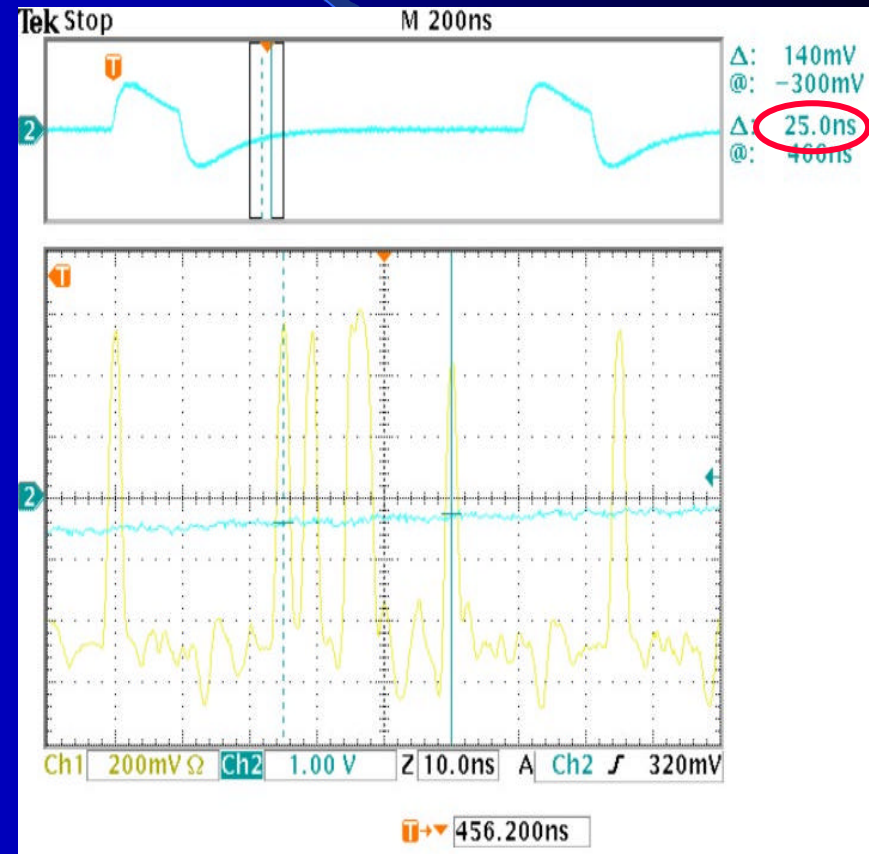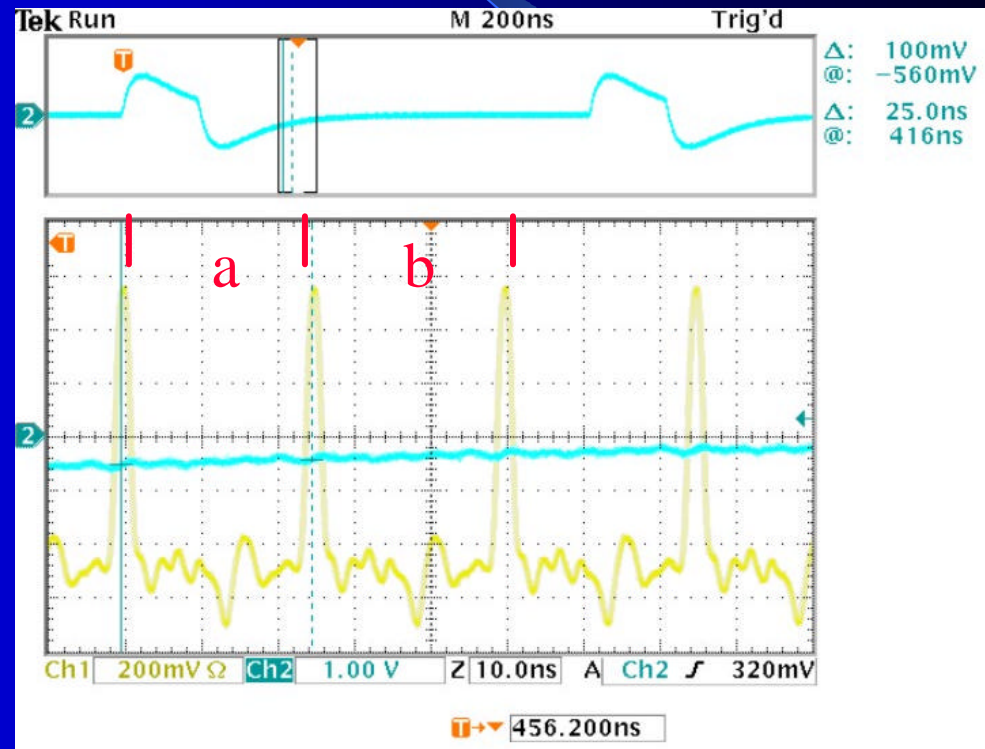
# LVDS Response (Cluster I)

# LVDS Response (Cluster I)

- Non-zero data in two consecutive time frames: BC-Mux

- Time frame a: 00_0100_1100

- Time frame b: 01_0000_0000

- Time frame b coincides with the non-zero data transfer on the jet/energy channel

# LVDS Response (Cluster II)

All data are zero for all time frames

# Summary and Interpretation

| LVDS channel | Parity Bit | BC-Mux | LVDS Data (LSB...MSB) |
|:---:|:---:|:---:|:---:|
| Cluster I (a) | 0 | 0 | 0100_1100 |
| Cluster I (b) | 0 | 1 | 0000_0000 |
| Cluster II (a) | 0 | 0 | 0000_0000 |
| Cluster II (b) | 0 | 0 | 0000_0000 |
| Jet/Energy | - | - | 01_0011_0000 |

- Wrong parity bit for all zero transmissions!
- Correct parity bit for all non-zero transmissions
- Correct BC-Mux bit allocation
- Jet/Energy data correspond to expectations (10-bit sum)
- All four MCM channels produce identical output

# Summary and Interpretation

- Parity error: K. Mahboubi found and corrected error in the Verilog code of the PPrASIC (CVS).
  New Synthesis and Layout necessary to fix error.

- Two test iterations were carried out. LVDS outputs differ only slightly (probably due to a different Phos4 sampling time of the input signal)

- All data are consistent with each other and follow PPrASIC specifications

# Summary and Interpretation

- Still no configuration access:
  relied on hardware default settings

- ADCs, Phos4, LVDS serializers and the AnIn are operating properly in default settings

- PPrASIC issues a BCID result within the specified time frame

- LVDS data transfer to crate system tested successfully

# Outlook I

- Setup the test system in the new KIP building

- Work on FPGA problems! Configuration of the chips on the MCM and MCM Testboard, readout of test data:
  - BCID coefficents
  - Phos4 configuration
  - ............

- Use video card as signal generator for MCM Testboard (Synchronization issue still needs work)

# Outlook II

- Read out and analyze LVDS output quantitatively

- Work on firmware and software to enable access to the serial interfaces of the PPrASIC

- Test more than one PPrASIC:
  - 2 MCMs were assembled at KIP
  - 3 MCMs to be assembled at HASEC
  - R. Achenbach: wafer test (using LabView)