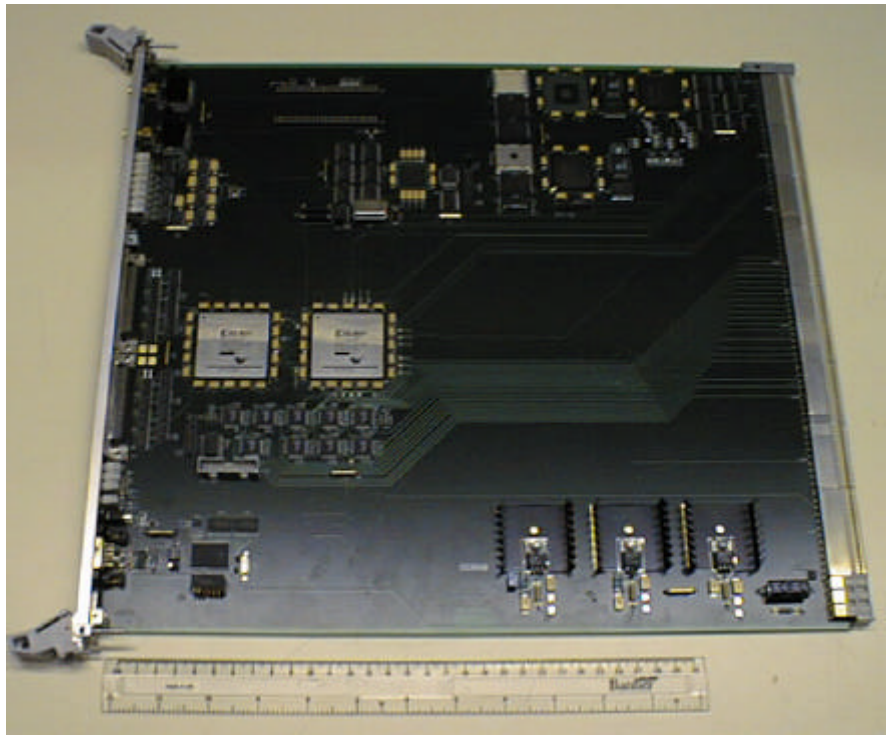
Common Merger Module, adapter modules and test cards: status & test plans

- Introduction
- Test equipment & RTM
- CMM tests: Real-Time Path
- CMM tests: Readout Path
- CMM tests: Automatic FPGA Configuration Logic
- Future Plans
- Summary

CMM: Introduction

- CMM merges data from CPMs and JEMs:
  - e/γ and t hit counts
  - jet counts
  - jet energy sums
- Most data processing done within 2 FPGAs (XCV1000E)
- Flash memories contain all required FPGA configuration files
- One CMM has been assembled.
- Error in Schematic prevents *auto*-config. of Crate FPGA:
  - OK for testing (JTAG config.) but will rework design before producing any more.
- Under test since spring.
- Test team: Panagiotis, Adam, Ian.



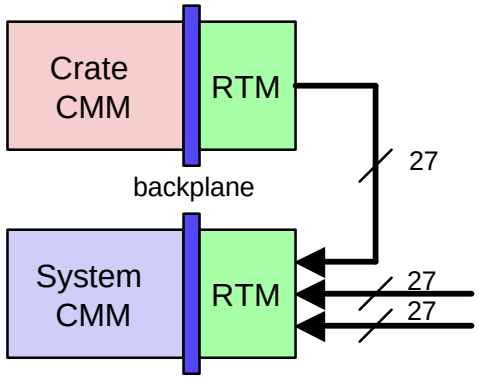
- what else to say here?

Test Equipment

- Equipment:
  - CMM
  - Processor backplane
  - DSS
    - GIOs to provide LVDS I/O
  - CPM emulator
  - RTM
- CMM, GIOs, CPM emulator & RTM were all being tested for first time.
- CPM emulator:
  - provided by Richard
  - takes LVDS signals from GIO Tx & drives LVCMOS→ backplane → CMM
  - works OK.
- Adam will speak about GIOs.
- RTM & CMM coming up....

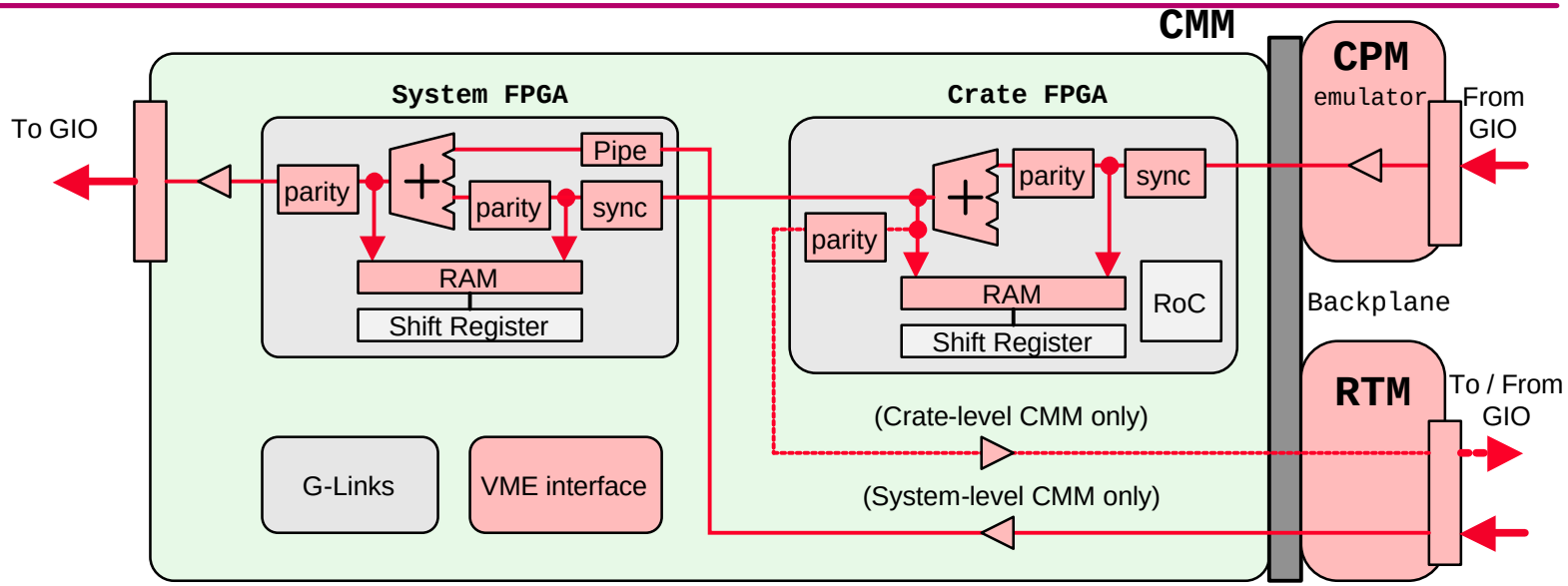
Rear Transition Module (RTM)

- Signals between Crate- & System-CMMs as differential LVDS on SCSI-3 cables.
- Signals pass to/from CMM, through backplane:



- RTM: passive module, maps signals from backplane pins to 3 SCSI-3 connectors.
- Fixed to back of crate using 2 horizontal, aluminium bars with guide slots.
- Four RTMs assembled July ‘02.
- One RTM tested: CMM ↔ RTM ↔ DSS GIO: all channels work.

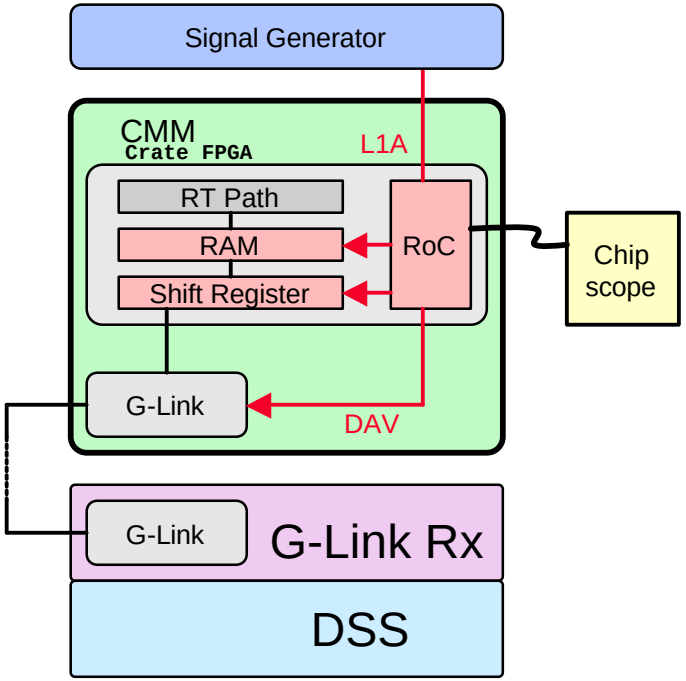
CMM tests: Real Time Path



- CMM versions tested: CP-System & CP-Crate
- Tested complete functional path through module
- Tested all IO channels to/from RTM, CPM & CTP (not concurrently)
- Used test patterns designed to expose functional & timing errors
- Used dedicated test firmware to provide extra data sources where necessary
- No soak tests (yet).

CMM tests: Readout Path

- Testing Readout Path is underway
- No TTC system available:
  - use Signal Generator to supply L1As on demand via TTC socket.
- All Readout Control signals on CMM examined via oscilloscope & chipscope: look good.
- *But* G-Link doesn't lock to G-Link on DSS.
- Investigating....



FPGA Configuration

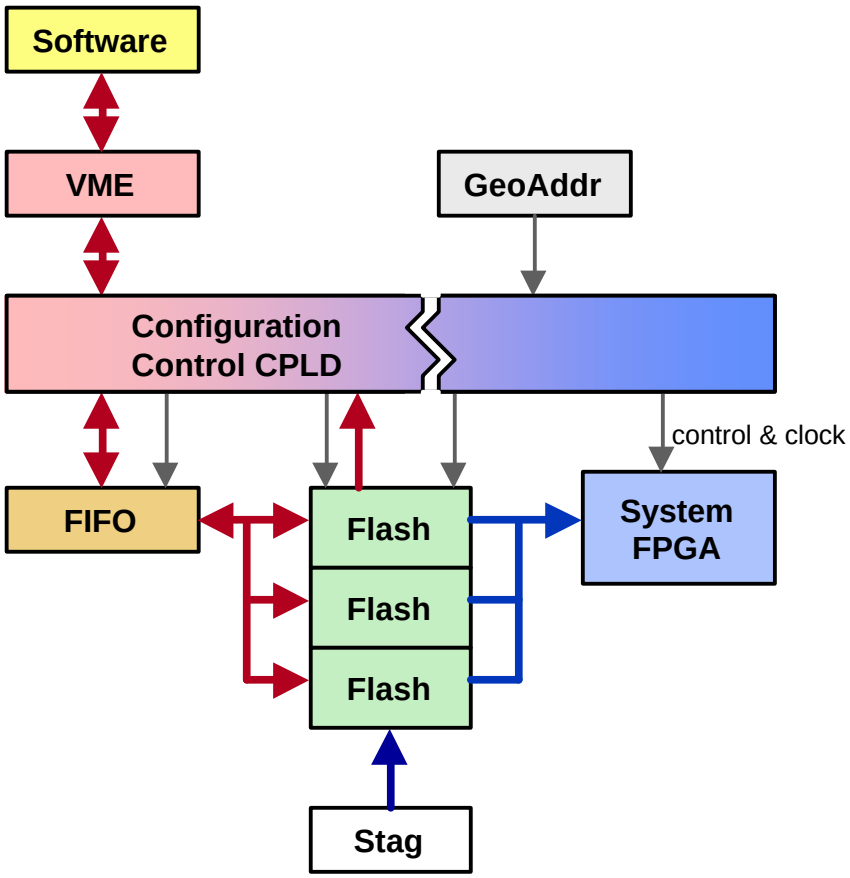
- Previously used JTAG to programme FPGAs.
- Now testing auto-config. logic....

Done:

- read & write data VME ↔FIFO
- load data FIFO → Flash
- read data VME ← Flash
- erase Flash from VME
- load data Stag Programmer → Flash
- programme Flash → FPGA

To do:

- programme VME→Flash →FPGA
  - problems fitting single CPLD design that can control all steps.
  - lacking front-end software
- load all 3 (System) Flash memories & test GeoAddr decoding



Future Plans

- Finish commissioning auto-configuration logic.
- Finish testing Readout Logic.
  - transfer data to DSS GIO Rx & check format is correct.
- Test with TTC.
- Aim: finish these tests by end of December.

- Start work on next CMM design:
- correct bugs found with current design
  - Crate FPGA auto-config
- *Possibly* upgrade VME interface & Config. Control CPLDs
- Aim: next CMMs ready for slice tests end of March ‘03.

Summary

- RTM tested & working.

- CMM testing:
  - Finished testing real-time path:
    - all I/O works;
    - complete slice through CP-merging hardware works (all possible paths).
  - Making progress testing CMM readout logic.
  - Making good progress commissioning FPGA-configuration logic.
  - Problems reworking designs in CPLDs:
    - VME Interface
    - FPGA Config. Control
    - may require device upgrade in next design iteration

- Plan to have next iteration of CMMs ready for slice tests in April.