CPM Test Progress

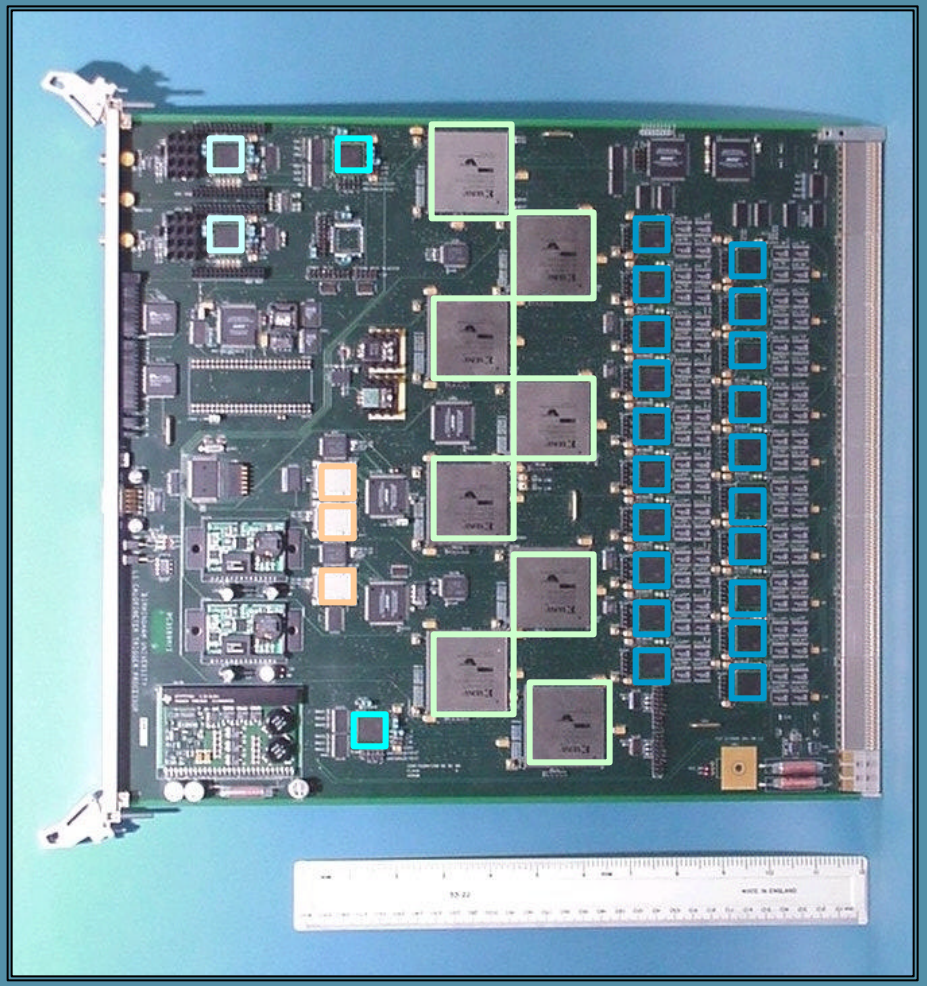
Steve Hillier

Gilles Mahout

Richard Staley

Firmware Status

- All downloaded and tested:
  - CP
  - Serialiser
  - Hit Merger
  - Readout Controller RoI and DAQ
- Fpga F/W downloaded per block via VME



Cluster Processor Chip

- Calibration process is working
- Algorithm OK, results double-checked with VHDL test bench
- Latency measurement:need extender board
- Data corrupted appears on 1 or 2 channels per chip:
  - Resolved by setting delays, via TTCrx chip, between CP chips and Serialiser, but with an headroom not bigger than 1.5 ns
  - Still under investigation with James (ChipScope)
  - New version CP chips F/W delayed due to new release of Xilinx S/W: problems with delay constraints

Serialiser Chip

- All working correctly:
  - Calibration pattern
  - Dual Port Ram access
  - FIFO filled on Level1A request
- To be tested:
  - LVDS input

Readout Controller DAQ & Roi

- Working correctly:
  - Dual Port Ram Access
  - Hit FIFO filled on L1A
  - Output on Glink port available with DAV signal
- On test:
  - Validity of data on Glink: delay problems between slices

Hit Merger

- Works correctly:
  - Id recovers
  - Hit correctly merged, output read via DPR of DAQ ROC
- To be tested:
  - Backplane output
  - Latency

Pre-integration tests

Tests	Materials	Status
LVDS	DSS + Lvds cards + cables	Already started
Backplane Real Time Data	DSS + GIO card + CMM emulator + Loop IO (extender) card	Coming soon…
Glinks	Logical Analyser	Already started

CPM Services

- All test done with stand alone program (I.e “../test/testcpmserv”)
- CPM Services use L1calo methods:
  - CPM: DaqModule (../modulesServices)
  - Srl,CP: DaqSubmodule
- Testvectors/Setting written from/to independent files:
  - Next step: uses L1calo database: first attempt successful

Next steps and Schedule

- H/W:
  - CPM tested near 80% completion (5 months) :
    - Stand alone test almost completed: CP-Srl path still under investigation: 2 weeks
    - External data sources just been added
    - Peripheral devices requested: 1-2 weeks + test: 1 week
- S/W:
  - Database integration: 2 weeks
  - Simulation package integration: 2 weeks
  - Low Level Run Control integration: 4 weeks
- ETA of a finished, not necessary polished, product: end November02?