CPM Prototype Hardware + related cards

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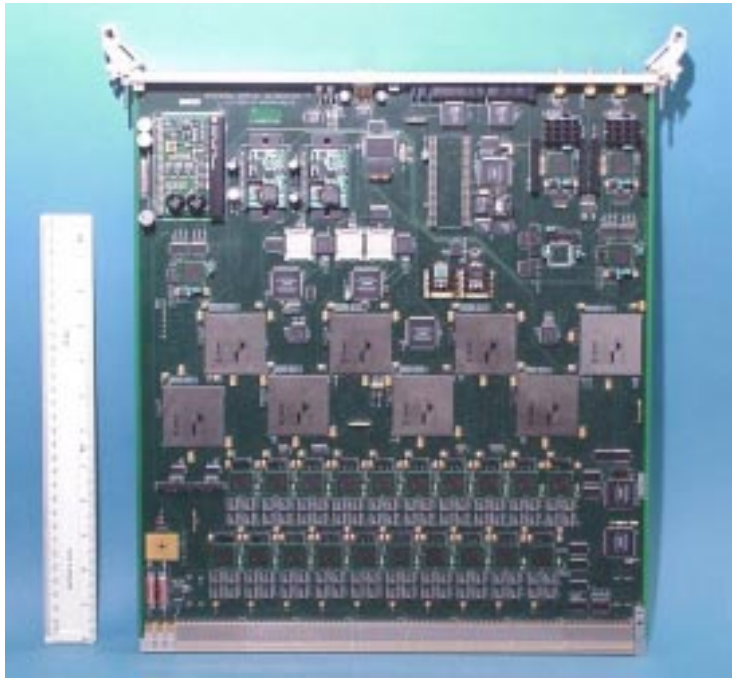
- Summary



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Progress (since last status report)

- All Serialisers , CP Chips , ROCs and HitSum FPGAs configure from FLASH memory
- Clock Distribution working with TTCdec.
- Transmission of 160Mb/s from Serialiser working (GM.) …

Surprises - TTCdec

I(We) expected a Version V3.0 TTCrx part, but discovered this doesn't exist! Actually using V2.2 device

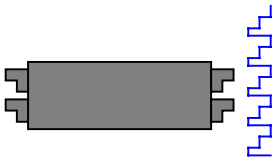
Implications for CPM.

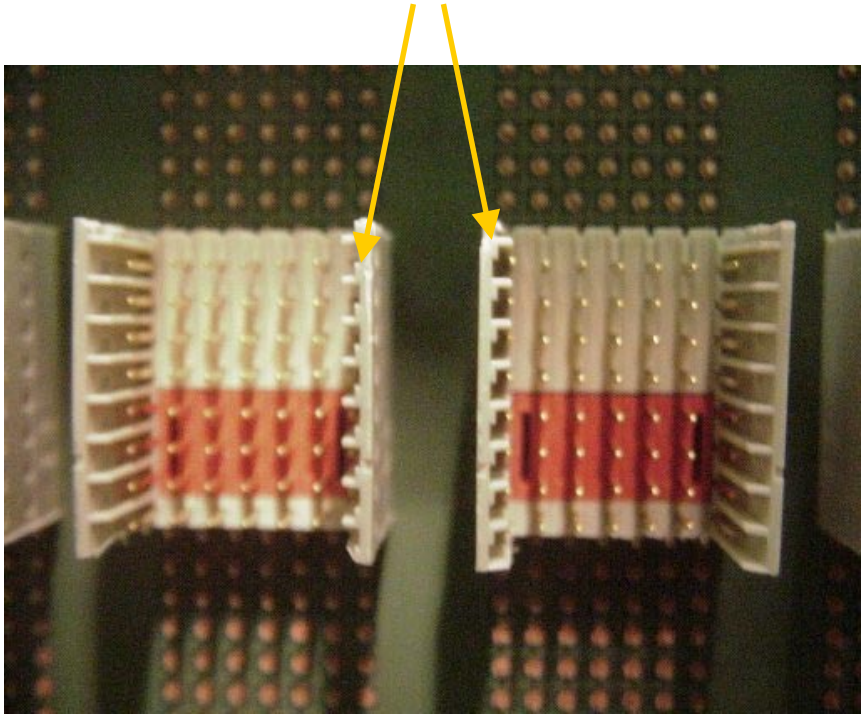
- No I2C → clock phase adjustment using TTC commands
- No Hardwired ID as PROM defines ID. → Geog. Addr ignored
- ERDUMP, CRDUMP and INIT are TTC broadcast commands.

New PCB for latest TTCrx being designed by RAL

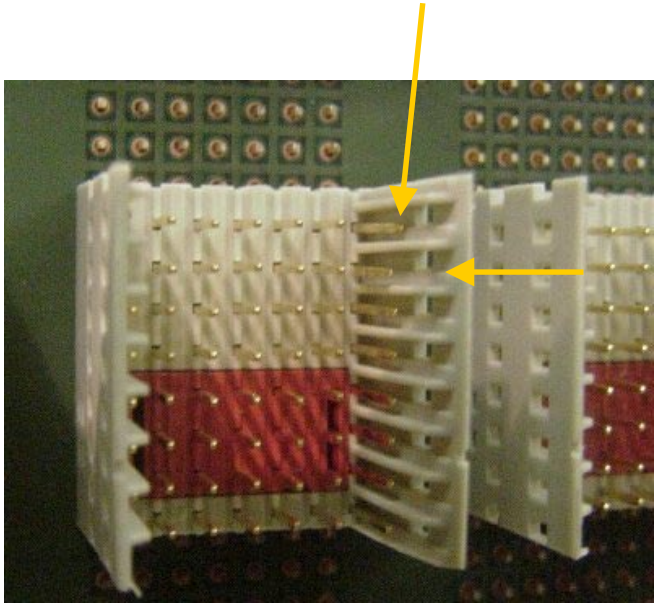
Surprises - LVDS Cable connectors

Cables are polarised, but orientation has not been specified.
Cable shrouds can (and have been) placed either way:



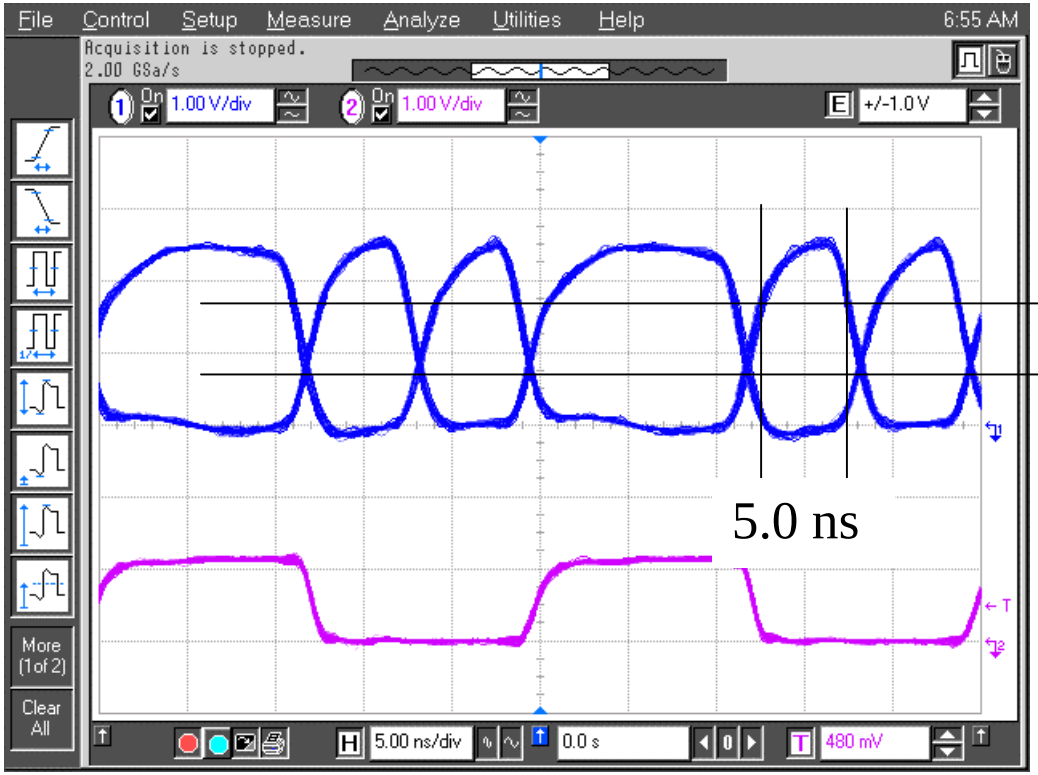


The outer columns of pins (z & f) interfere with the cable connector and become permanently bent:



160 Mb/s Links

Typical CP chip input:



1.7V V_{ih} CMOS2 thresholds

0.7V V_{il}

Present 160Mb/s links use signals with a large voltage swing:

Virtex-E outputs
Not enough drive for 2.5V CMOS2 signals on transmission lines.
LVTTL outputs do have the current drive, but voltages swing 3.3V.

Should consider redesigning CPM , Serialiser and CP Chip to allow lower-voltage signalling standards:

- Reduced noise
- Reduced power consumption.

480 x 21mA ≅ 10A!

The lower V.swing standards require CP FPGAs connected to low-noise voltage reference.
Not possible with existing CPM - different pin-out.

Mechanical

- PCB is too flexible , concerned about BGAs.

- CP Chip Heatsink were glued on to package (after JTAG test).
  - must be removable for rework.

Both defects will be corrected on next PCB.

Further Assembly

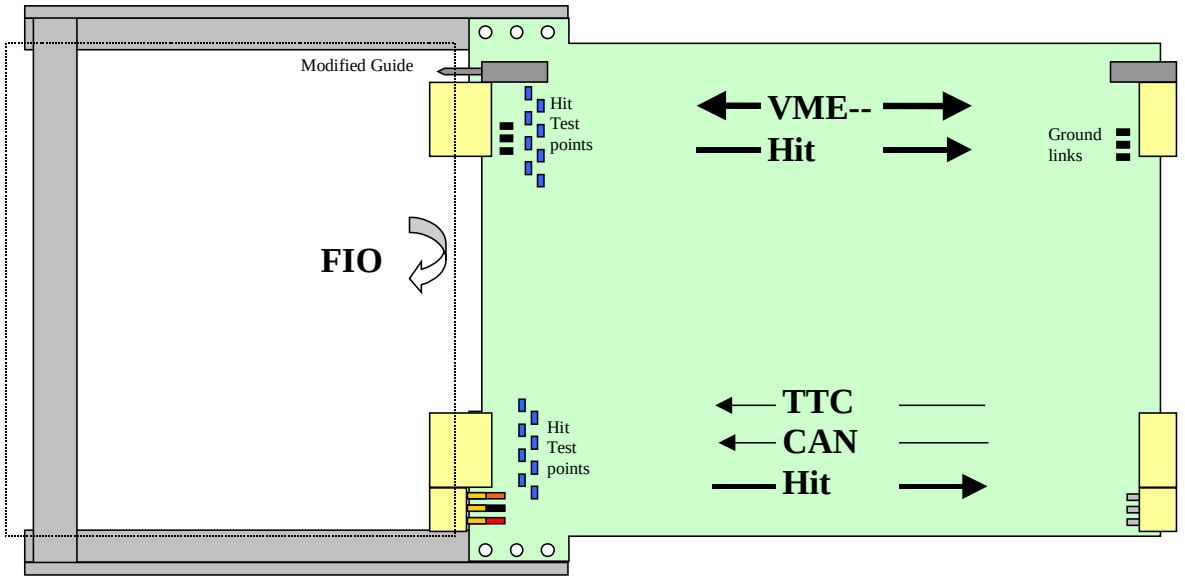
More tests especially connectivity before CPM #2 assembled.

- LVDS receivers functioning
- LVDS connection to Serialisers
- Backplane I/O
- Test ROCs and Glink output
- Test Hit Sum FPGAs and output to CMM slot

Expect to make decision before end November.

Other Cards - Crate Extender

- VME , Hit outputs , TTC and CAN.
- + CMM position.
- Loopback FIO at module connector. All FIO signals.



http://www.ep.ph.bham.ac.uk/user/staley/CPM_Extender.pdf

2 Assembled PCBs expected 8th November.

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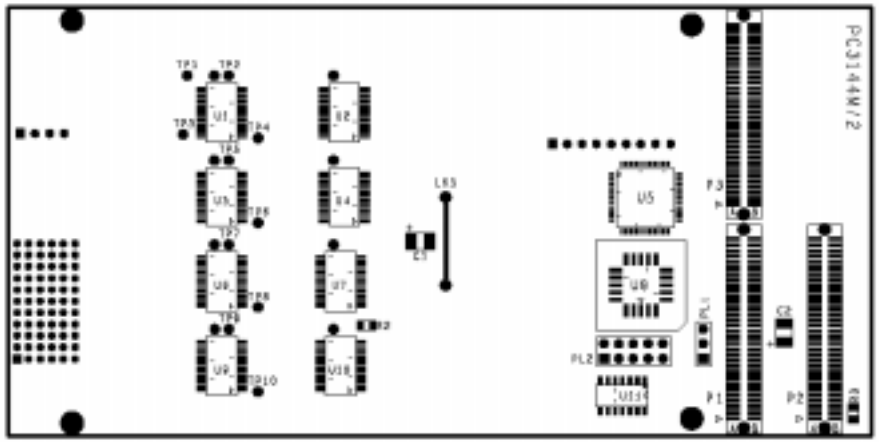
Other Cards - LVDS Source for DSS

- AMP Connector to match AMP compact cable assembly.
- Cable pre-compensation R + L.
- JTAG EEPROM.



http://www.ep.ph.bham.ac.uk/user/staley/DSS_LVDS_3_1.pdf

5 Assembled PCBs expected 8th November.

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Summary(1/2)

Still making steady progress with CPM testing.

- Reliable access to FLASH memory
- FPGA configures from FLASH memory
- TTC system operational
- Onboard 160Mb/s transmission working.

Summary(2/2)

Have not yet found anything to prevent CPM design from being used in Slice-Test, but …

Further connectivity tests needed before CPM #2 assembled. Decision End November.

Waiting for Crate Extender. Will provide better access to CPM .