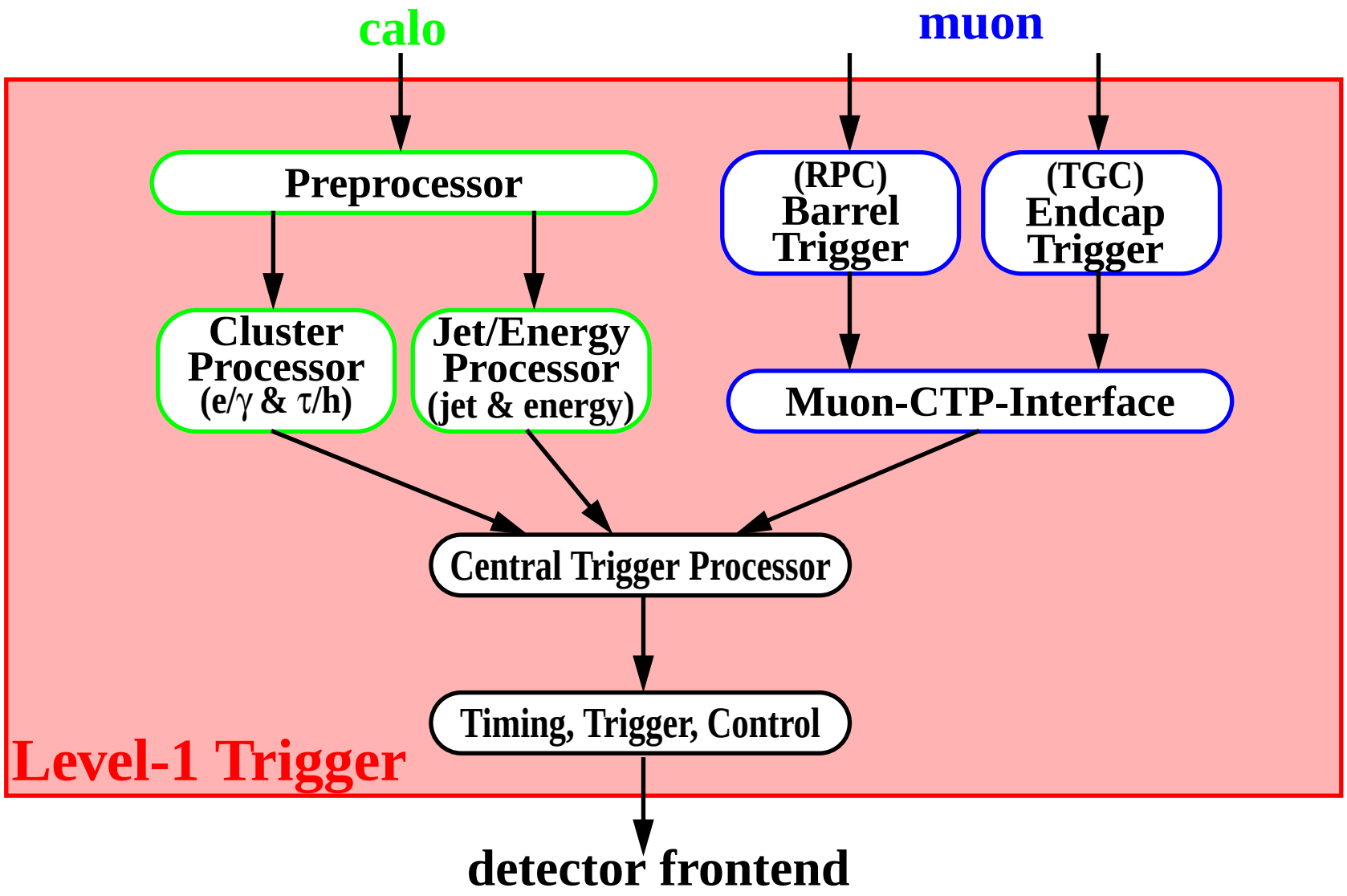
Integration of the Central Trigger Processor Demonstrator

- **with the Muon-CTP-Interface:**
  - Setup
  - Results
- **with the Level-1 Calorimeter Trigger:**
  - Programmable Patch Panel
  - Software
  - Planning

N. Ellis, Y. Ermoline, P. Farthouat, K. Nagano,
T. Schörner-Sadenius, G. Schuler, R. Spiwoks, T. Wengler

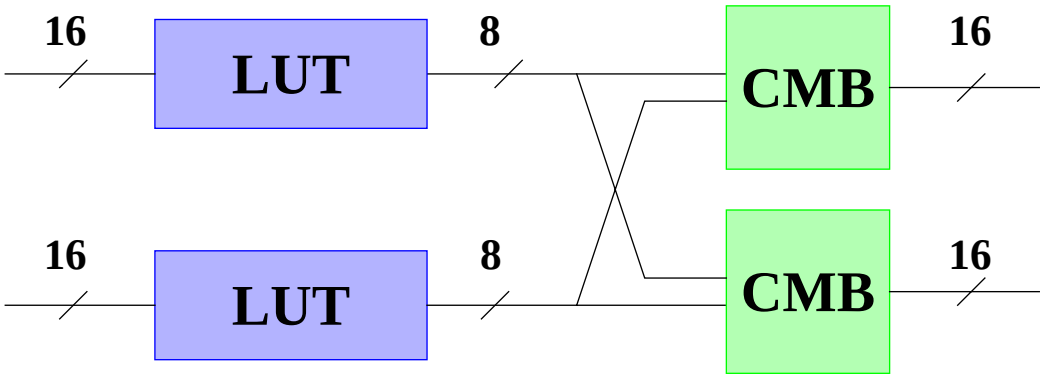
Level-1 Trigger - Overview



CTPD - Overview

→ EDMS ATL-DA-ES-0005:

- trigger inputs: **32** bits ⇒ trigger items: **32** bits



- synchronization: BC or !BC; alignment: 1 to 24 BC
- test memory: 1 MWords or random generator (32 independent bits)
- monitoring: event sampling, scalers, temperature/voltage
- no ROD functionality!

• Modules:

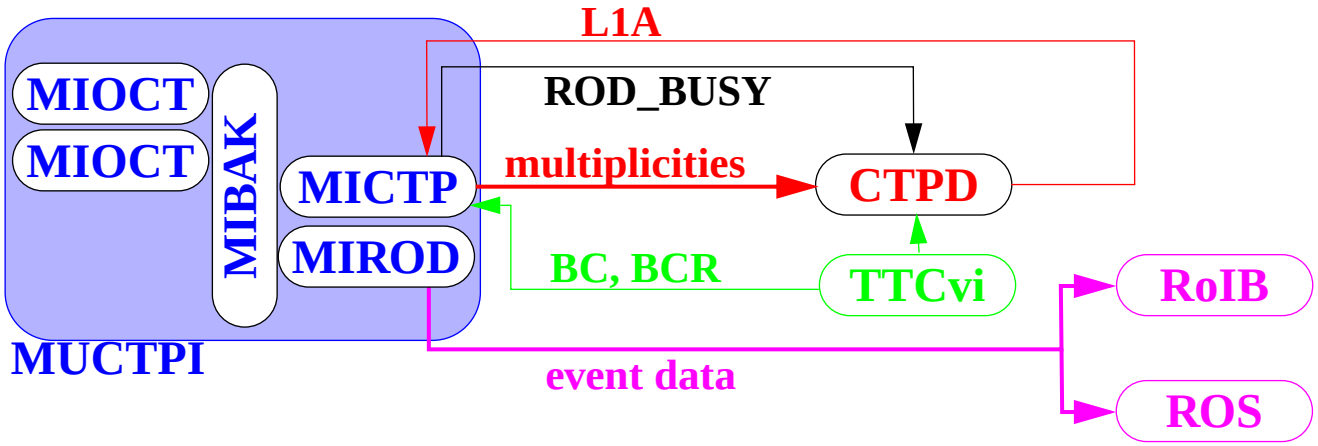
→ 1996, 2 modules 9U VME(32):

module #0: Altera Max7000 on sockets

module #1: Altera Max7000S in-situ programmable

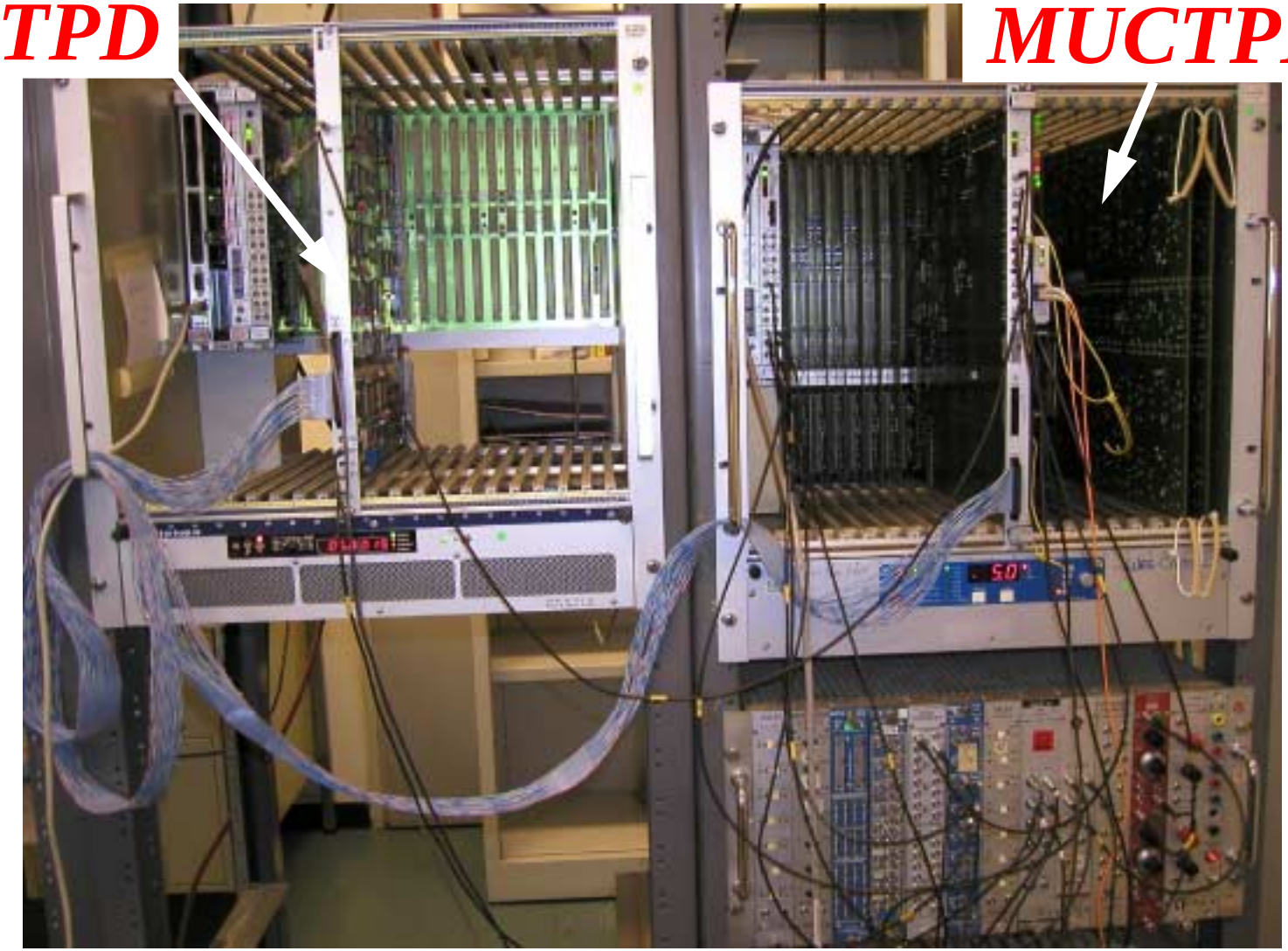
Integration MUCTPI → CTPD (1)

→ presented at LECC 2002 in Colmar, France



- **MUCTPI:**
  - generate multiplicities from test memory in (two) MIOCTs
  - send multiplicities to CTPD and receive L1A from CTPD
  - send event data to Level-2 (RoIB) and DAQ (ROS)
    and send ROD_BUSY to CTPD if required
- **CTPD:**
  - receive multiplicities and generate L1A
  - monitor trigger input in monitoring FIFOs (VMEbus)
- **TTCvi:**
  - generate common BC and BCR (+ test signal for test memory of MIOCTs)
- **RoIB and ROS:**
  - emulated by PC: receive (+ verify) event data

Integration MUCTPI → CTPD (2)



Integration MUCTPI → CTPD (3)

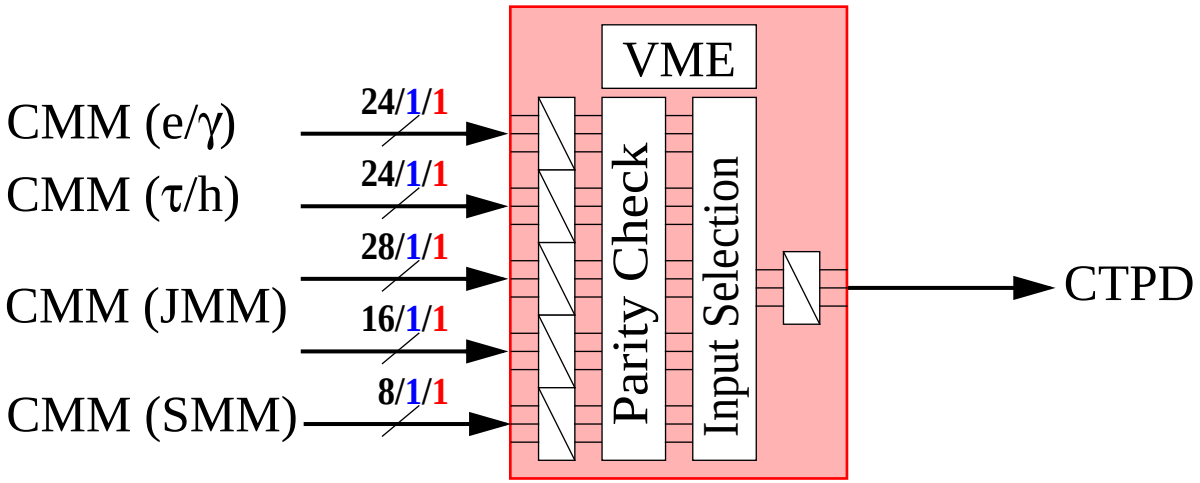
- Phase Measurement:
  - measure on CTPD the phase of the clock which accompanies multiplicities:
    precision ≈ 1.5 ns
  - latch multiplicities safely on CTPD:
    window width ≈ 20 ns
  - position CTPD clock to minimize L1A latency:
    latency ≈ 55 ns
- Data Integrity:
  - read the multiplicities from CTPD's monitoring FIFO (VMEbus):
    no error in ~ 10^9 events (running for a few hours)
- Flow Control:
  - use MUCTPI's ROD_BUSY to throttle generation of L1A:
    works up to ~ 1 MHz L1A frequency
- Conclusion:

  MUCTPI and CTPD were successfully integrated!

  ⇒ CTPD ready for integration with Level-1 calorimeter trigger!

  but what needs still to be done?

Programmable Patch Panel (Y. Ermoline)



⇒ total input signals: **108 trigger inputs + 5 clock + 5 parity**

- internal groups (clock fan-out): 25 × (**4 trigger inputs + 1 clock)**
- output selection to CTPD: 8 × (**4 trigger inputs + 1 clock)**

→ status: analog multiplexers* do not work at 40 MHz!

***ADG706 16:1 analog mutliplexer from Analog Devices**

⇒ build mezzanine boards with new multiplexers

⇒ available by end of 2002

→ to do early 2003:

- develop low-level software for control and monitoring
- test!!! ... with DSS modules ???

Software for CTPD

- ROD Emulation:
  - read from CTPD monitoring FIFO, format event data, send to S-Link
  - use ROD Crate DAQ dataflow task (ROS software)
  - first tests (reading and sending) indicate: about 30 kHz event rate

- Trigger Menu Handler:
  - demonstrator trigger menu handler (EDMS ATL-DA-ER-0002)
  - new trigger menu compiler (compatible with Athena, T. Schörner)

  what flexibility of the trigger menu is required?
  ⇒ can we put everything in LUTs?

- Run Controller:
  - to be developed: use ROD Crate DAQ run controller (ROS software)
    → will include control of patch panel
    → configuration data mostly in local files with ad-hoc format
    attempt integration with configuration database later!

Planning for Integration

- Time:

  When? For how long?

- Test Programme:

  1) Time-in calorimeter signals:

  → Programmable Patch Panel + phase measurement on CTPD

  2) Generate L1As and check data integrity:

  → trigger menu, monitoring on CTPD
  comparison with input data ???

  3) Read out CTPD and build full events:

  → ROD emulation + Run Controller

- Hardware:

  → open questions concerning:

  - 9U VMEbus crate (P0!)
  - TTC and ROD_BUSY modules
  - S-Link Cards
  - ancillaries (scope etc.)