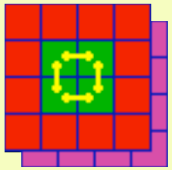


Sunnybrum and Rainybrum:
Birmingham, 7–9 November 2002

- Personal view, not a comprehensive summary of all that was presented and discussed.
- Apologies for anything important that's missed — tell me.
- If you think anything is mistaken or objectionable please say so!

- Categories are as follows:

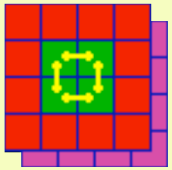
  + (mainly) positive development, or something that has been sorted out, or simply good progress.

  – negative development, or something that needs to be sorted out that may cause problems, or an item where work seems to have stopped — no criticism of people involved is (necessarily) implied.

  ◆ More work or a decision is needed.

  ! controversial point that must be discussed further.

- No names mentioned since it's very difficult to be fair to everyone who has done all the work — people will know who they are!



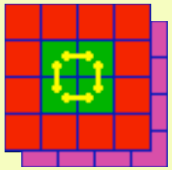
'Executive summary'

+Lots of progress

+No showstoppers …
(yet!)

–Timescales,
timescales, □
timescales ...

–We must now take milestones and schedules very seriously; ATLAS is not always going to be 5 years away!



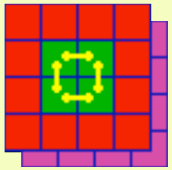
Physics simulation

+ Offline trigger simulation very close to finished
+ Validation in progress, no major problems so far
+ 'Analogue' simulation, such as noise and time history of pulses, is starting

– Who carries on the work long-term? (Also said last time)
– Would be a lot easier and quicker if things were stable in the offline computing world

+ Promising results on possibilities of triggering on invisible Higgs

• But trigger on 2 jets + missing-E_T not presently in trigger menu



Calorimeter signals and cables

- TileCal receivers still not specified
- Documentation of connections from calorimeters still not finished

- Should buy long TileCal cables soon
- Must buy TileCal receiver amplifier chips as soon as possible
- Consider small-scale test of calorimeter signals with front-end electronics in test beam in 2003

Preprocessor

+ ASIC tests so far look quite promising; other chips and cards also looking good

◆ But a lot remains to test on ASIC

– Re-assessment of delays and effort levels indicate that Preprocessor and ROD modules for slice test will be delayed by ~9 months compared to our recently agreed timetable

– MAJOR EFFECT on our TEST PROGRAMME!

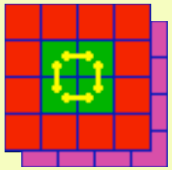
– Still big shortage of effort

◆ Try to recover some of the delay by reducing effort needed or doing it outside, e.g. board layout

! Perhaps use CP/JEP ROD?

◆ Re-think testing: do more with CP and JEP subsystem and system tests before adding Preprocessor to system

+ Very cooperative, open-minded approach to minimising the problems



CPM and JEM

+ Much testing done on CPM; so far some small problems but nothing serious
+ Will get second module (with minor fixes) made, probably starting end November
+ Online software for CPM progressing well

+ Much work done to understand and improve JEM firmware, both energy and jet; now integrated
+ More cooperation between Mainz and Stockholm
+ JEM test vectors from physics!
+ Much testing done on JEM0, should go to RAL soon
+ JEM 1 design progressing

◆ Finish JEM 0 documentation
◆ Must decide whether to make two more JEM0s if JEM 1 is too far away in time

! JEM 1 makes logical changes in chip families to raise processing capacity, but the board has become very demanding to make. Must be reviewed!

Common modules and backplane

+ CMM testing going well; so far so good
+ Second module with minor fixes should be ready for tests

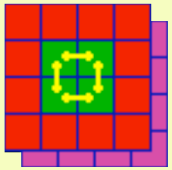
+ TCM, GIO, TTCrx cards all in nice shape
+ Further progress on debugging and firmware for CP/JEP ROD prototype; flow control bug finally found
+ Backplane only has a few minor problems

– Final backplane must have robust polarisation of cable connections
– CERN standard crates probably ok for RODs, but for PPr, CP and JEP there ! may be problems with the dense cable arrays at the rear — must be checked urgently

◆ Use a simple (web-based) system for problem reporting, not just random emails

◆ Order at least one VME and perhaps one other crate now

Try to avoid a custom crate solution, or at least try to use standard crate even if we need a custom power supply arrangement



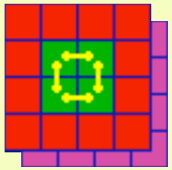
DCS, calibration and joint tests

+ Clean option of one PCI card to handle DCS in all our crates *(but needs Windows PC)*, Fujitsu per module, with possibly Fujitsu + ELMB linked by SPIbus on TCM
+ Good calibration contacts and meetings now set up with calorimeters, and calibration document written
+ Proposal for very useful test-beam work (not all needing beam) with calorimeters and other parts of T/DAQ in 2004 still very much alive
+ Seems useful to do *limited* work using front-end electronics with calorimeters in 2003
+ Local Trigger Processor proposal has potential to solve some of our problems ...

! Is it useful to have a CPU or some other processor on a PPr ROD daughter card, to do some of the calibration?

◆ Carefully consider scope of our involvement, especially in 2004 run

◆ ... but we need to provide feedback so that it meets out needs



Online software

+ Good contacts established with the rest of level-1
+ Simulation of Preprocessor started
+ JEM software changing from shell scripts to HDMC and module services, and adding features

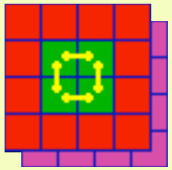
– Need to document Preprocessor readout format

+ First release of online software package — nice demonstration done showing big advances
+ HDMC bugs fixed, progress on various modules
+ Lots of progress on simulation, many new features and more modules
+ Databases now being used seriously

– Serious shortage of effort on the software continues, and this is delaying some hardware and firmware testing!
– Comparison with timetable of last meeting shows *many achievements*, but not as soon as predicted

! Try to get non-software experts to do as much module testing as possible (also said this last four times); s/w now more mature and should be tried

◆ Carry on with work towards multi-slice readout, timing calibration, more complex tests, multi-module setups, etc.
◆ Comprehensive list & table of what's missing was shown



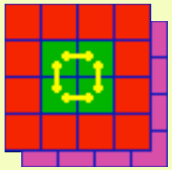
Tests and timescales

+ Nice work being done to prepare CTPd for tests

+ New schedule attempting to handle new problems proposed; has some good flexible features
+ Longer subsystem phase in UK with CP and JEP

– Were already slipping a bit on the July timescale
– Our new problems are real and cannot be easily worked around — slippage is ~9 months
– Production and commissioning phases now VERY compressed
– We MUST improve our ability to stick to timescales, which are now incredibly tight!

◆ Must keep better informed about progress, problems, etc. than at present



Summary

+ People are being very open about problems as well as successes

+ There has been a lot of progress on the hardware, and no serious problems have appeared so far!

– ... But also new and very serious slips in timescale, and continuing shortage of effort

Thank you to the Birmingham group for a productive, well-organised meeting in attractive surroundings!