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Jet/Energy Module

-firmware status-

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Jet/Energy Module

- Firmware status -

- What has happened since Stockholm
  - Code clean-up
  - Simulation of the complete RTDP
  - Implementation of Readout Controller
    - Tests and Simulation of ROC Coding
  - Merging of Jet Algorithm and Energy Code
- Outlook

What has happened since Stockholm …

Overview:

- Continued tests of the RTDP which included
  - E_X and E_Y tree (see Jürgen‘s talk)
  - Playback and Spy etc.
  - TTC interface – communication between Control_FPGA and all of the other processor FPGAs
  - Code clean-up ….
    - Control_FPGA **(Spartan II XC2S200-6-FG456)**
      - Number of SLICEs 106 out of 2352 4%
      - Maximum frequency: **78.858MHz**
    - Input_FPGA **(Spartan II XC2S200-6-FG456)**
      - Number of BLOCKRAMs 13 out of 14 92%
      - Number of SLICEs 1006 out of 2352 42%
      - Maximum frequency: **42.450MHz**
    - MainProcessor **(Virtex E XCV600E-7-FG680C)** **- NO JET! -**
      - Number of SLICEs 1677 out of 6912 19%
      - Number of BLOCKRAMs 40 out of 72 55%
      - Maximum frequency: **41.642MHz**
    - Readout_Controller **(Spartan II XC2S200-6-FG456)**
      - Number of SLICEs 246 out of 2352 10%
      - Maximum frequency: **69.560MHz**

Simulation of the complete RTDP

The used testbench for this simulation includes all RTDP components from the Input FPGA and MainProcessor implementation except for the input synchronisation

⇒ *this means*:

odd parity check – outmask – presummation for elm/had channels – comparison with a low threshold – multiplexing – demultiplexing – calculation of E_t, E_X and E_Y – saturation

One example:

• All 8 Input FPGAs were filled with a random pattern (maximum value 64) which was based on adder tree for Fast Trigger Simulation.

JEMResult_3.txt

1	209	19	211
2	178	17	180
3	273	26	276
4	313	30	316
5	199	18	201
6	184	17	186
7	231	22	233
8	237	22	239
9	304	29	307
10	183	17	185
11	211	20	213
12	268	26	271

SIM_SUM_3.txt

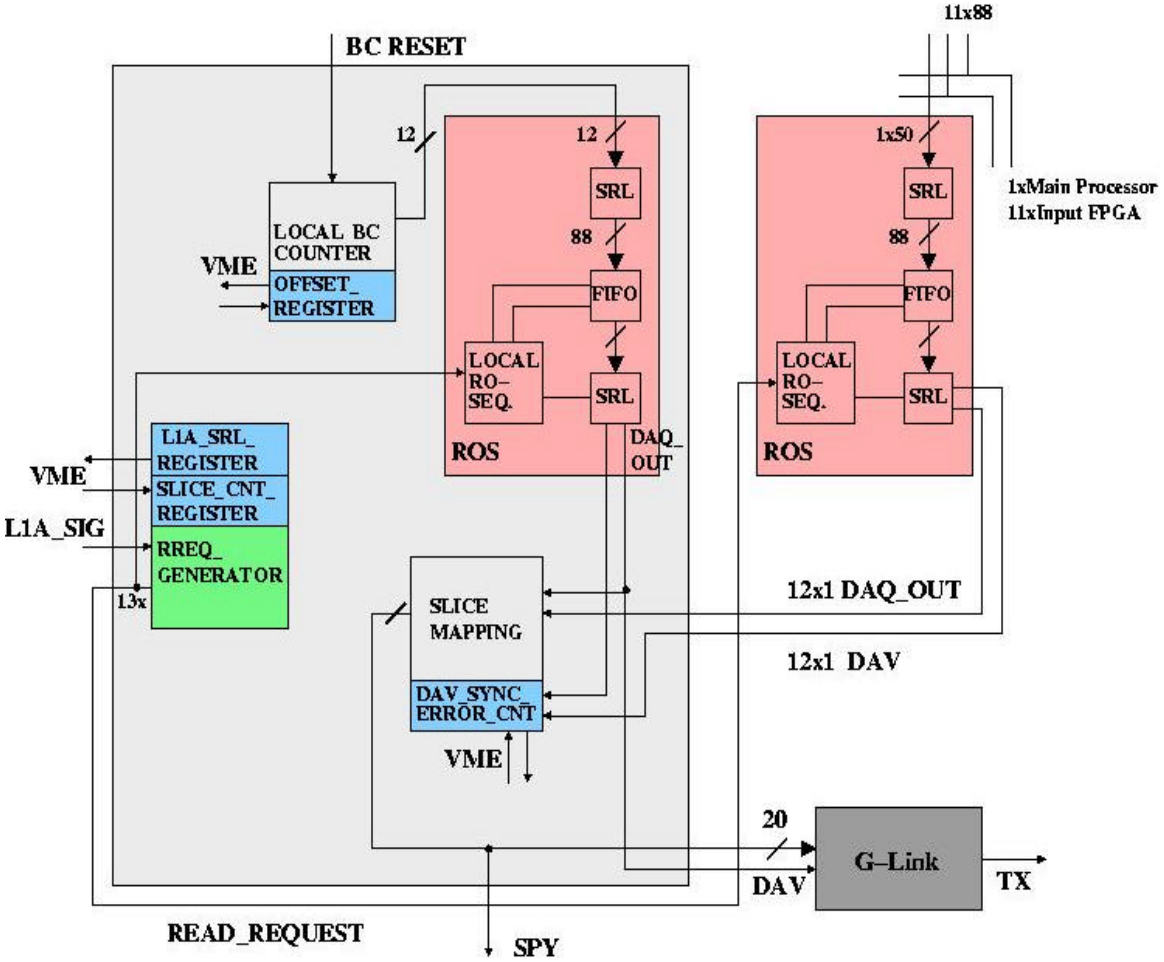
1	0	0	0
2	0	0	0
3	0	0	0
4	0	0	0
5	0	0	0
6	0	0	0
7	0	0	0
8	209	19	211
9	178	17	180
10	273	26	276
11	313	30	316
12	199	18	201
13	184	17	186
14	231	22	233
15	237	22	239
16	304	29	307
17	183	17	185
18	211	20	213
19	268	26	271

Conclusion:

• Agreements of both results (software and hardware simulation)

• Estimation for current latency : about 7 clock cycles + 2,5 clock cycles due to the input synchronisation

Implementation of readout controller



- RoC controls and reads out local RoS which located in the processor FPGAs
- An additional RoS that is implemented in the RoC captures the bunch crossing number, which is generated by a local counter
- VME registers set delay of the readrequest signal, the count of slices and offset for the BC counter
- RoC maps all of the incoming single data bit streams in an according format
- Spy memory is implemented for debugging purposes
- **NOTE**: Readout of Jet RoIs is realized in a similar manner

ROC implementation is simulated and tested (on board via spy) successfully!

Integration of Jet Algorithm in the framework of the Energy Code

The current version of the code includes the interface for the jet algorithm and the additional implementation of :

- **All registers (threshold + size) according to the documentation**
- **Spy functionality for the jet multiplicities**
- **DAQ path for the ROI readout (- previous formats -)**

Preliminary estimation of the required resources after place and route:

Current target: Virtex XCV600E-7-FG680C

Device utilization summary:

Number of External GCLKIOBs	1 out of 4	25%
Number of External IOBs	463 out of 512	90%
Number of LOCed External IOBs	0 out of 463	0%
Number of BLOCKRAMs	48 out of 72	66%
Number of SLICEs	**6910 out of 6912**	**99%**
Number of DLLs	1 out of 8	12%
Number of GCLKs	2 out of 4	50%

Design statistics:

Minimum period: 35.216ns (**Maximum frequency: 28.396MHz**)
Maximum net delay: 14.704ns

The device doesn‘t match the requirements!

JEM 0.2: Virtex XCV1600E-6-FG680C

Device utilization summary:

Number of External GCLKIOBs	1 out of 4	25%
Number of External IOBs	463 out of 512	90%
Number of LOCed External IOBs	0 out of 463	0%
Number of BLOCKRAMs	48 out of 144	33%
Number of SLICEs	7506 out of 15552	48%
Number of DLLs	1 out of 8	12%
Number of GCLKs	2 out of 4	50%

Design statistics:

Minimum period: 31.029ns (**Maximum frequency: 32.228MHz**)
Maximum net delay: 13.791ns

One critical point may be the maximum frequency! (see Attila‘s talk)

Outlook

Jem0.0 - Jem0.2:

- **Simulation of the input side of TTC_handling (Control_FPGA)**

  (=> TTC_Interface between Control-FPGA and all the other FPGAs is already tested via VME and operates successfully)

- **Expansion of the present RTDP testbench to integrate the jet algorithm**

Common Merger Module (CMM):

- **My main task will be to write and simulate firmware for the RTDP of the Energy Common Merger Module!**