The Jet Algorithm

ATLAS Level-1 Calorimeter Trigger

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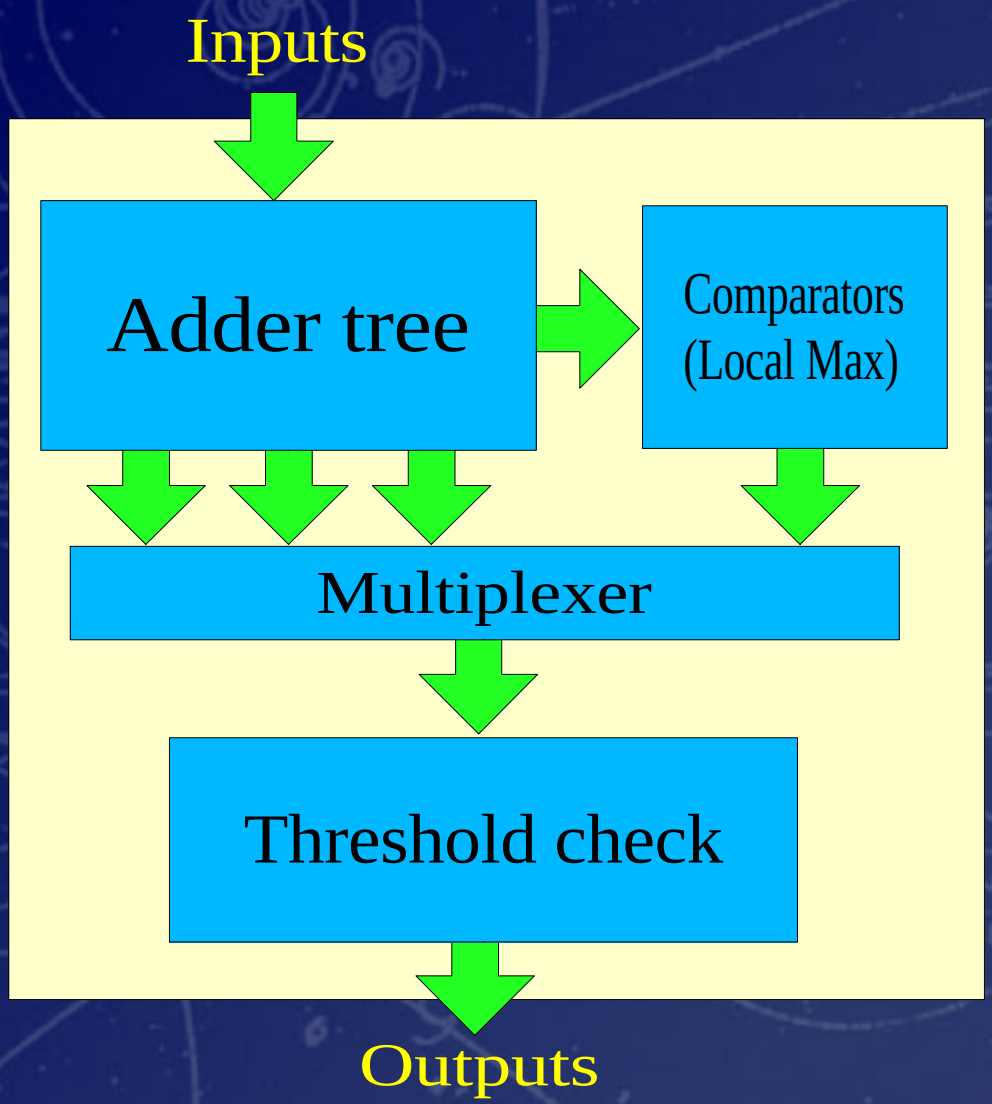
Recent Progress on Jet Algorithm

- Improved speed
- Removed bugs
  - In algorithm
  - In test bench software
- Standalone tests of algorithm on FPGA
- Integration into JEP FPGA firmware

Design


Inputs
Adder tree
Comparators
(Local Max)
Multiplexer
Threshold check
Outputs

Speed improvements

- **Problem:** after place-and-route, the algorithm did not work at 80 MHz.
- **Solution:** key parts had to be redesigned:
  - Overflows are checked during next clock cycle.
  - Convert comparators in local max finder and threshold check to 12- or 11-bit parallel (Overflows added to cluster sums).
  - Long data path through multiplexer split in half with FFs to increase clock speed (but extra latency added)
- **Result:** design now works at 110 MHz
  - But: extra half-tick of latency added

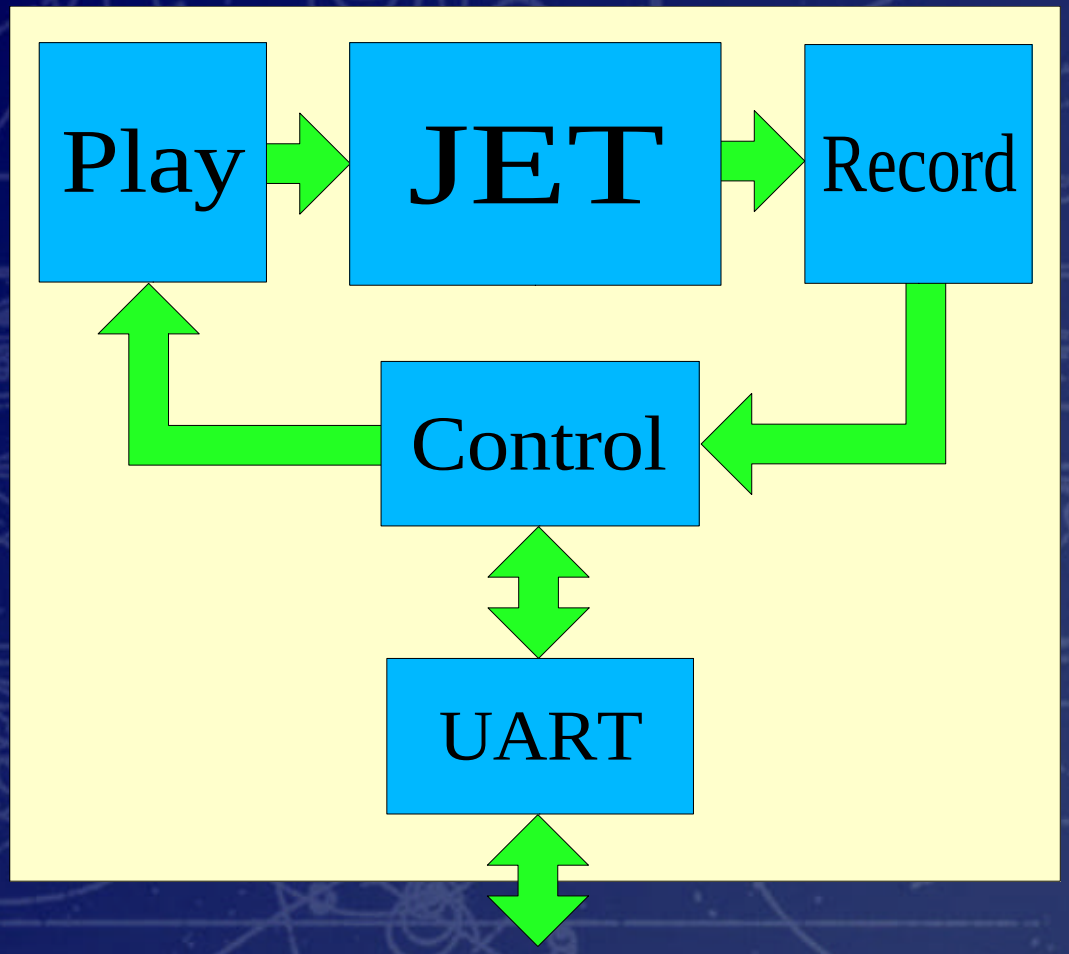
Bugs found and removed

- Algorithm
  - Small errors in local maximum finder.
  - Phase selection throughout the whole design has been corrected.
  - Some wrong connections have been corrected.
- Test Bench
  - All the signals (including the 40 MHz clock) are delayed relative to the 80 MHz clock to avoid problems with Modelsim.

Standalone tests of algorithm

- VHDL simulation
  - Simulation of the result from the synthesis.
- Tests on Virtex II developer board
  - RAM blocks for playback and spy memories
  - Loading, control and readback using RS232
  - Results.

Algorithm tests on VirtexII board



Integration into JEM firmware

- Some minor modifications to the JET-algorithm interfaces with rest of JEM firmware.
- The VHDL code for the Jet-algorithm has now been integrated into the main processor FPGA code for the JEM.

Outlook

- Continue to test and debug the current algorithm until satisfactory performance on prototype JEMs.
- Begin work on other firmware relevant to Jet data path and ROI readout.
- Assist in software development for testing and operating the JEP
- Testing TTC functionality of JEP