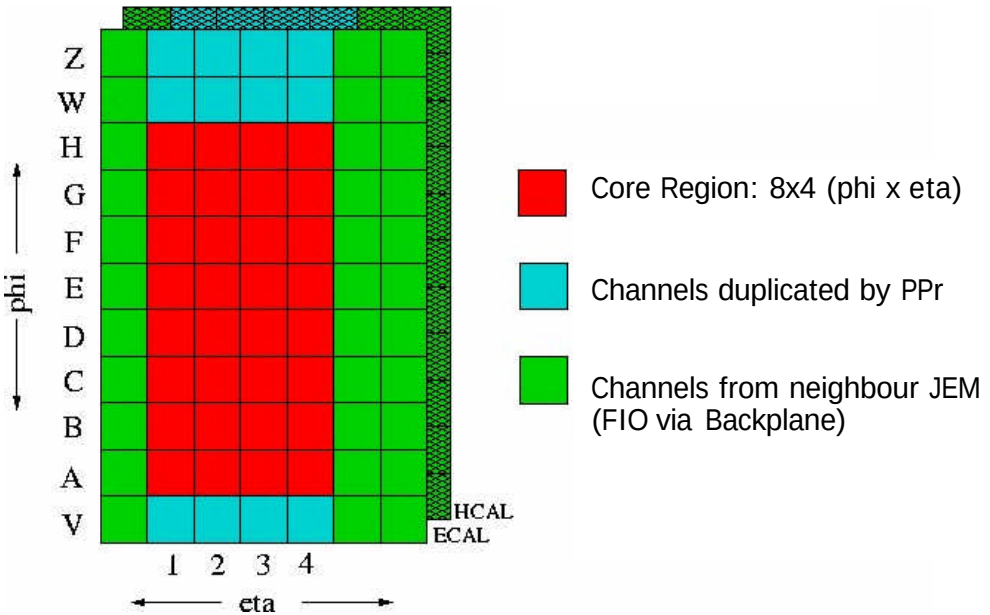
Jet/Energy Module: Prototype Tests and Test Vectors

- Test Vectors for Energy Summation on JEM
  - Types, Production and Usage
- Test Results:
  - standalone JEM Tests
  - JEM Tests with LVDS data input from DSS
- Outlook

Test Vectors: JEM Input Mapping

- Validate correct function of Real-Time Data Path in Firmware (algorithm, control path and memory implementation) and Hardware (connectivity, mapping)
- Generate appropriate input data stream and check results from Module by comparing simulation to readback from JEM



Data Inputs to JEM Algorithms:
11 x 7 (phi x eta)
For Energy sums: Only core region (red)

Test Vectors: Implementation

- Based on 'old-style' Fast Trigger Simulation by Kambiz, Alan, Rolf et. al., Fortran Linux version available on:
  `http://butler.physik.uni-mainz.de/~mahboubi`
- Adder Tree based on implementation into fast trigger simulation by Rolf Dubitzky for complete JEP
- Modified code: generate data for single JEM in a 2-crate JEP, match firmware implementation w.r.t. saturation and multiplication (via LUTs), quad-linear encoding on sum outputs
- Two data source options for module tests:
  - Playback memories in InputFPGAs (depth: 256) for all 8 InputFPGA used in sum algorithms - 64 channels (phi x eta x em/had: 8x4x2)
  - Data Buffers on DSS (depth 32k), only 2 InputFPGAs - 16 channels (phi x eta x em/had: 2x4x2)
- Data sink: Spy memories in MainProcessorFPGA (depth: 256)

Test Vector Types (1): Physics

- Two options of Test Vectors available for JEM prototypes (JEM 0.0/0.1/0.2), both use simple ASCII ‚Standard Output‘
- Physics data: tt → WW → 4 jets, from PYTHIA and ATLFAST with fast trigger simulation
  - very high mass-bin (700-2000 GeV) and pT-bin settings in PYTHIA (> 500 GeV)
  - Simulation originally for whole JEP. For single module tests: find occupied JEMs in JEP with Sum-ET > 64 GeV
  - Library of 2.5 Mio Events (10000 Files, 255 Ev. each) produced
  - All PYTHIA 5.7 channels available if needed

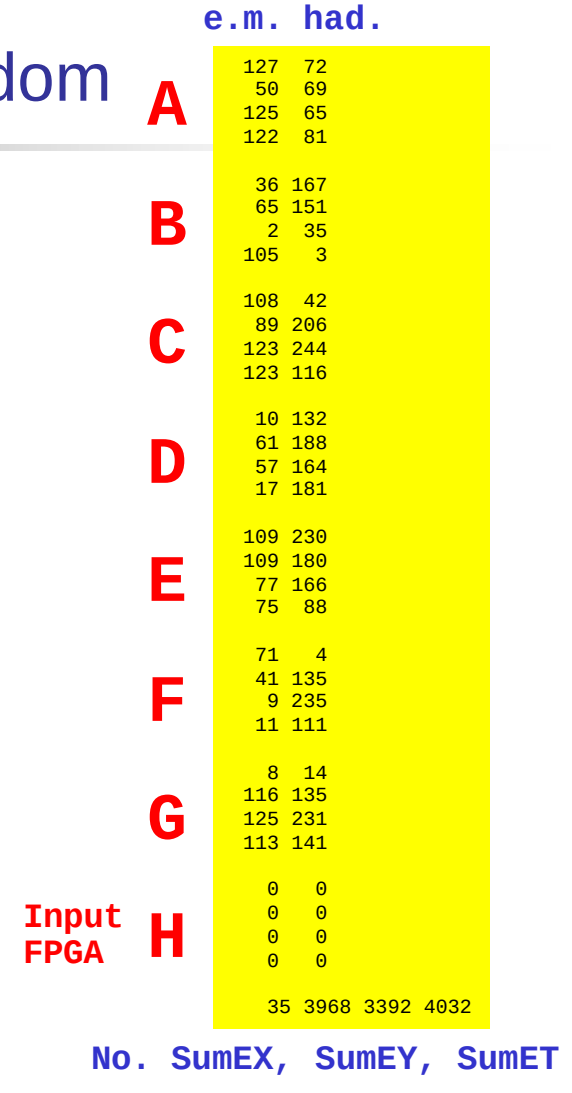
Input FPGA

	e.m.	had.
A	0	0
	0	1
	0	59
	0	1
B	0	1
	2	3
	4	9
	1	5
C	0	1
	3	6
	49	247
	9	6
D	0	0
	7	3
	60	115
	12	6
E	0	0
	1	0
	9	10
	0	2
F	0	0
	0	0
	0	0
	0	0
G	0	3
	0	0
	0	0
	0	0
H	0	0
	0	0
	0	0
	0	1

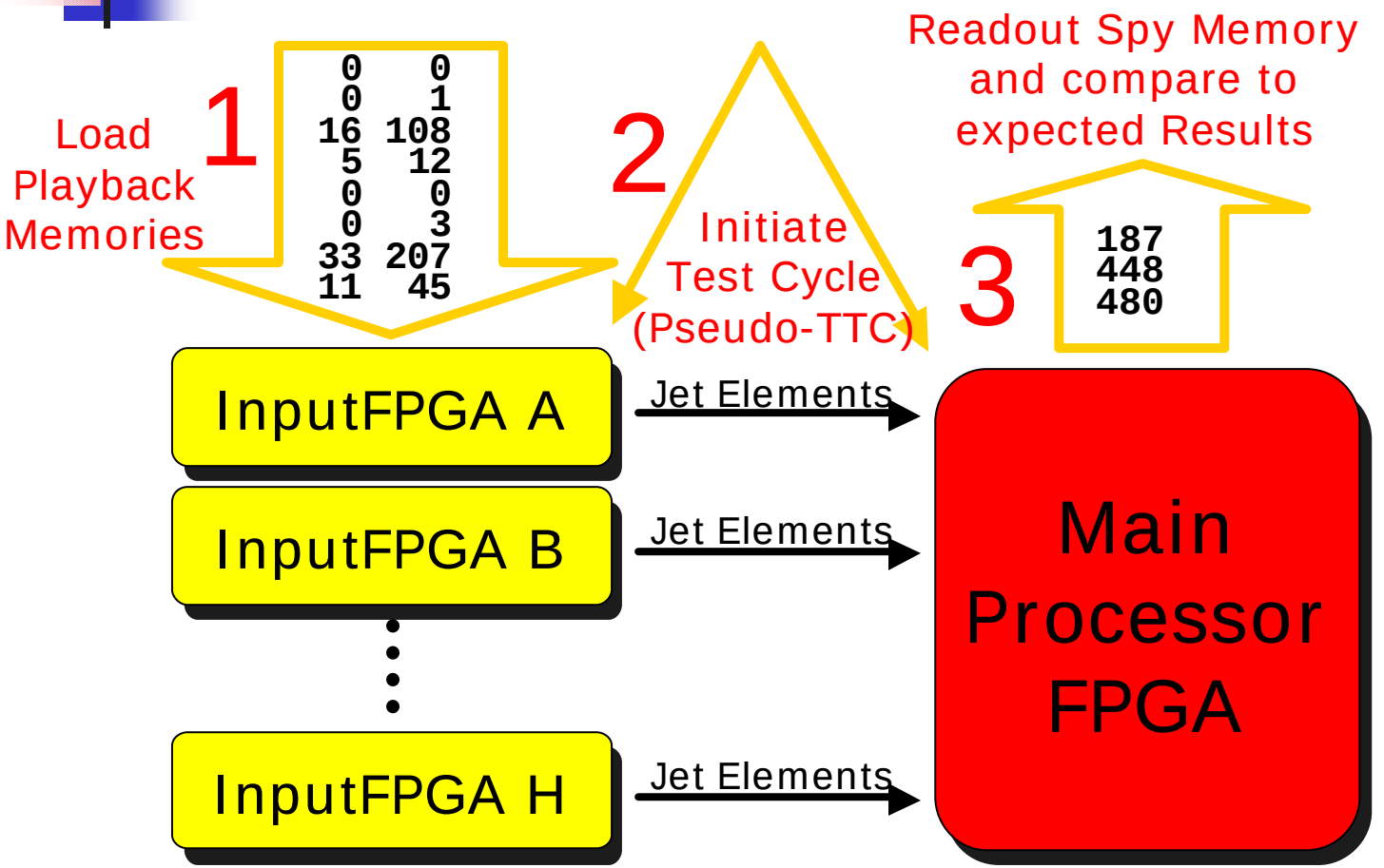
No.	SumEX	SumEY	SumET
	18	528	304	624

Test Vector Types (2): Random

- Random patterns: Each JEM Input (e.m. or had. channel before summation to Jet Element) filled with random data.
  - Use complete data width (0-511 GeV)
  - Make sure the values are really random (random seed modification)
  - Need to avoid saturated adder trees (not much knowledge gained...)
  - Other options for basic connectivity tests exist, others - like single channel scan - can be easily included due to ‚standard' test vector format



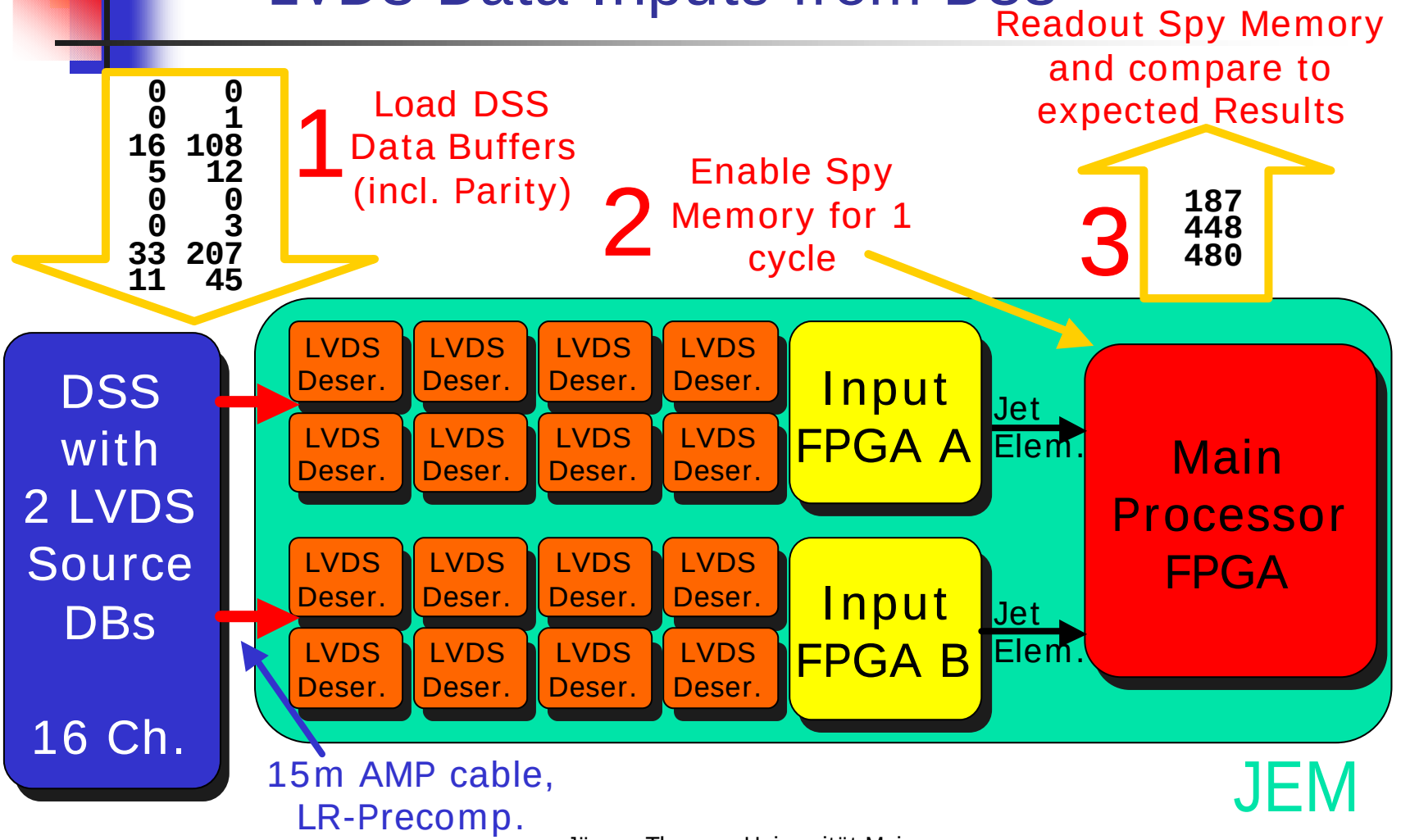
Standalone Energy Summation Test



Stand-alone Test Results

- Random Patterns (JEM 0.0 and JEM 0.1):
  - 6 Mio. Events have been processed
  - All Sum-ET, Sum-EX and Sum-EY results are identical to the expected values from the simulation
- Physics Data (JEM 0.1):
  - 60 Mio. Events (24x tt test vector library) have been processed
  - All Sum-ET, Sum-EX and Sum-EY results are identical to the expected values from the simulation

Energy Summation Test using LVDS Data Inputs from DSS



DSS-JEM LVDS Interconnection Mapping

- DSS with 2 LVDS Daughterboards sources 16 LVDS channels, able to feed 2 InputFPGAs on JEM with data, using simple adaptor
- Connecting cables (AMP) are 4 Ch. per assembly, but backplane has alternating LVDS input rows
- DSS originally designed for 20 Bits (G-Link), LVDS Serialisers use upper or lower 10 bit halfword of buffer filling
  - All this causes fairly complex mapping of DSS data buffers to JEM Input channels

DSS->LVDS->JEM0 Input Channel Mapping

2 DSS LVDS Source Daughtermodules + MZ-Cable-Adapters
Upper Slot Daughtermodule: Cable 1 (top), Cable 2 (bottom)
Lower Slot Daughtermodule: Cable 3 (top), Cable 4 (bottom)
JEM0: Backplane Connector JB4, InputFPGAs E+F
Cable mapping (starting from top of backplane - VME conn.): 1,2,3,4

DSS Data Buffer No.		InputFPGA		Link Channel		
0x20000	**1**	No.		No.	?	
	[9:0]	5	F	4	1h	
	[19:10]	6	E	4	1h	
0x40000	**2**					
	[9:0]	5	F	0	1e	
	[19:10]	6	E	0	1e	
0x60000	**3**					
	[9:0]	6	E	1	2e	
	[19:10]	5	F	1	2e	
0x80000	**4**					
	[9:0]	6	E	5	2h	
	[19:10]	5	F	5	2h *	*Bit 7 buggy*
0xa0000	**5**					
	[9:0]	5	F	6	3h	
	[19:10]	6	E	6	3h	
0xc0000	**6**					
	[9:0]	5	F	2	3e	
	[19:10]	6	E	2	3e	
0xe0000	**7**					
	[9:0]	6	E	3	4e	
	[19:10]	5	F	3	4e	
0x100000	**8**					
	[9:0]	6	E	7	4h	
	[19:10]	5	F	7	4h	

Test Results: LVDS Data Inputs from DSS

- Random Patterns for two neighbouring InputFPGAs (A+B, C+D, E+F, G+H), full data range (0-511 GeV)
  - Continues data stream input from DSS, random test patterns loaded into data buffers, resync'ed LVDS links
  - Spy Memory in MainProcessorFPGA has depth of 255, match output to expected results stream (DSS buffer memories are 32k deep)
- Simultaneous test works only with random data from same daughter board (either 1/2 e/h or 3/4 e/h) with other daughter board sending only constant values (DSS timing/sync ?)

- 1.8 Mio. Events have been checked
- All Sum-ET, Sum-EX and Sum-EY results are identical to the expected values from the simulation
- LVDS data transmission is stable, All tests performed on JEM 0.1

Outlook

- Energy summation tests on JEM prototypes have been successfully completed using onboard memories
- JEM tests with LVDS data inputs from DSS have been performed
  - Need to Investigate reason for data stream mismatch of different LVDS Source Daughterboards
- Now repeat tests on new JEM 0.2
- Repeat tests with Input Synchronisation