

# JEM SOFTWARE

Thomas Trefzger

Jürgen Thomas, Cano Ay, Marc Unverzagt

University of Mainz, Germany

# EXISTING SOFTWARE

- Configure FPGAs
- Load DSS buffer memories
- Load and read playback, spy memory
- Load, read and write, compare test vectors

Problem: Shell scripts directly calling VME driver utilities

# FRAMEWORK

- 2 Concurrent CPUs with either VME LINUX or CERN VME driver
- PC with RedHat Linux 7.3

All existing software is running with both drivers on all CPUs.

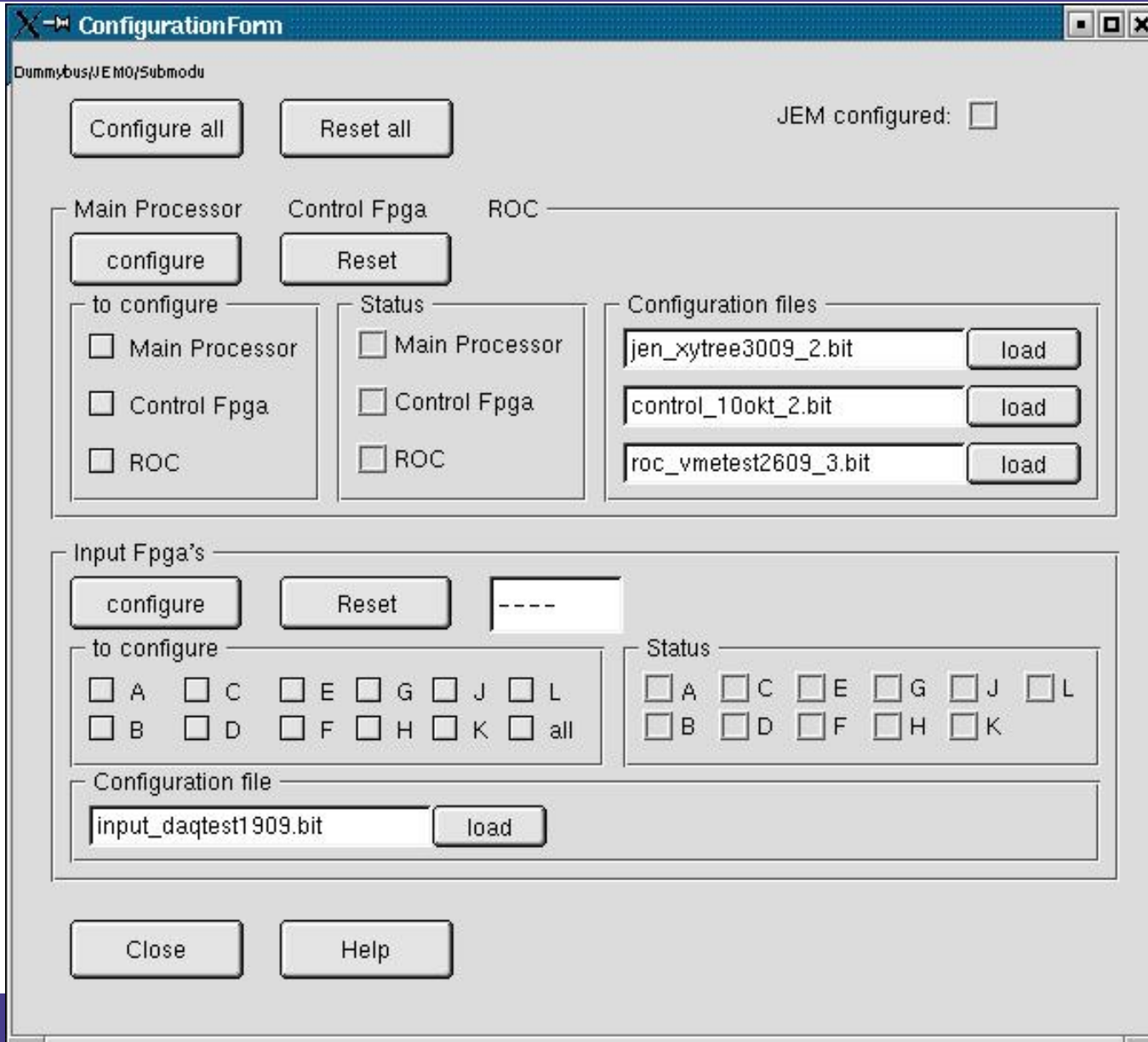
On all CPUs the relevant software packages are installed (ATLAS online software, HDMC, CMT, CVS,...)

# PROBLEM...

Using a different VME driver means  
rewriting existing software...

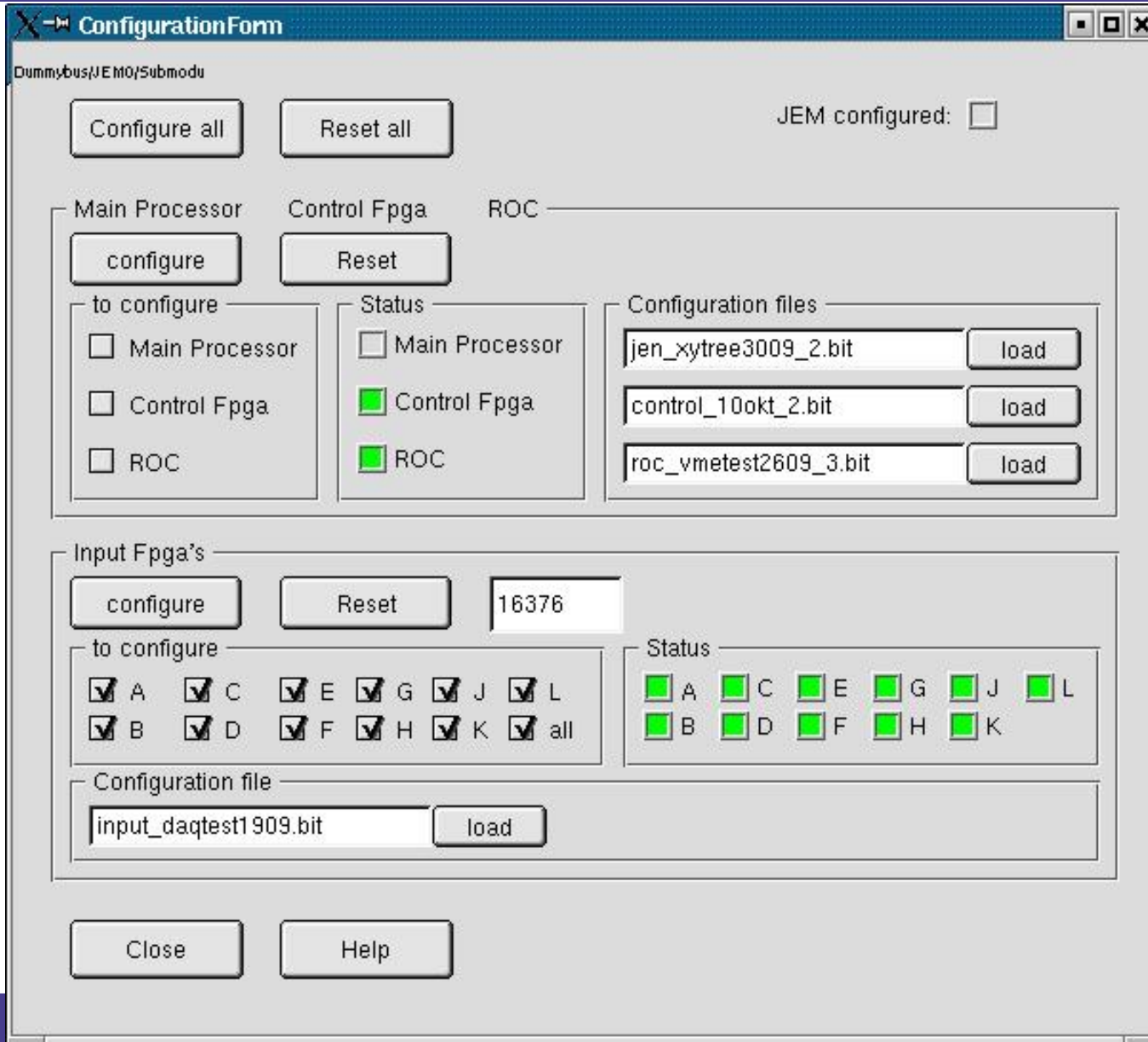
Simple shell scripts are not an elegant  
solution...

# SOFTWARE MODULES (HDMC)



Cano Ay, new PhD student:  
Started with Gilles FpgaXilinxJEM file,  
Program to configure control FPGA, main processor and ROC

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# REGISTERS (HDMC)

Hardware Diagnostic, Monitoring and Control System (Version 0.2)

File Scripts Parts Windows Help

dummyjem2919.parts	Init. State	Attributes	State String
[-] Dummybus	accessible		""
[-] JEM0	accessible	0x00fc0000	""
[-] ControlFPGA	accessible	0x2000	""
[-] ROC_FPGA	accessible	0x4000	""
[-] MainProc_(JEm)FPGA	accessible	0x6000	""
[-] InputFPGA-V-(L)	accessible	0x8000	""
[-] InputFPGA-A-(K)	accessible	0xA000	""
[-] InputFPGA-B-(J)	accessible	0xC000	""
[-] InputFPGA-C-(H)	accessible	0xE000	""
[-] InputFPGA-D-(G)	accessible	0x10000	""
[-] InputFPGA-E-(F)	accessible	0x12000	""
[-] InputFPGA-F-(E)	accessible	0x14000	""
[-] InputFPGA-G-(D)	accessible	0x16000	""
[-] InputFPGA-H-(C)	accessible	0x18000	""
[-] InputFPGA-W-(B)	accessible	0x1A000	""
[-] InputFPGA-Z-(A)	accessible	0x1C000	""
[-] VME_CPLD	accessible	0x0	""
[-] Submodule_offset	accessible	0x1	""
[-] XilConfigJem	accessible	motherboard	""

View Name

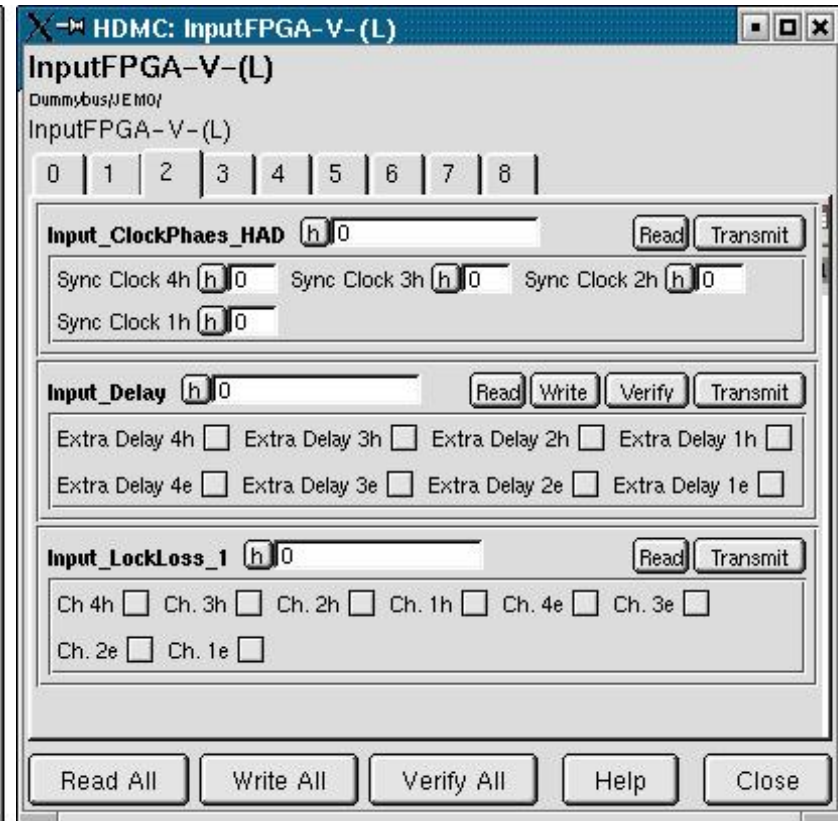
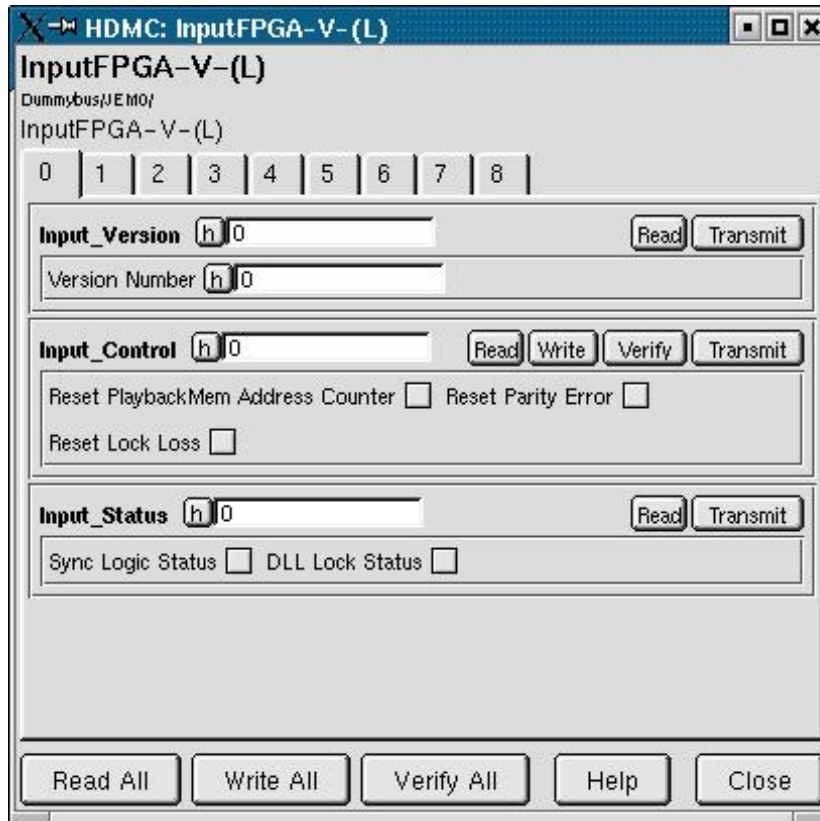
Part: Assembler  
Create Part

View: Create  
Create View

Connections

Help  
Exit

# INPUT FPGAs (HDMC)

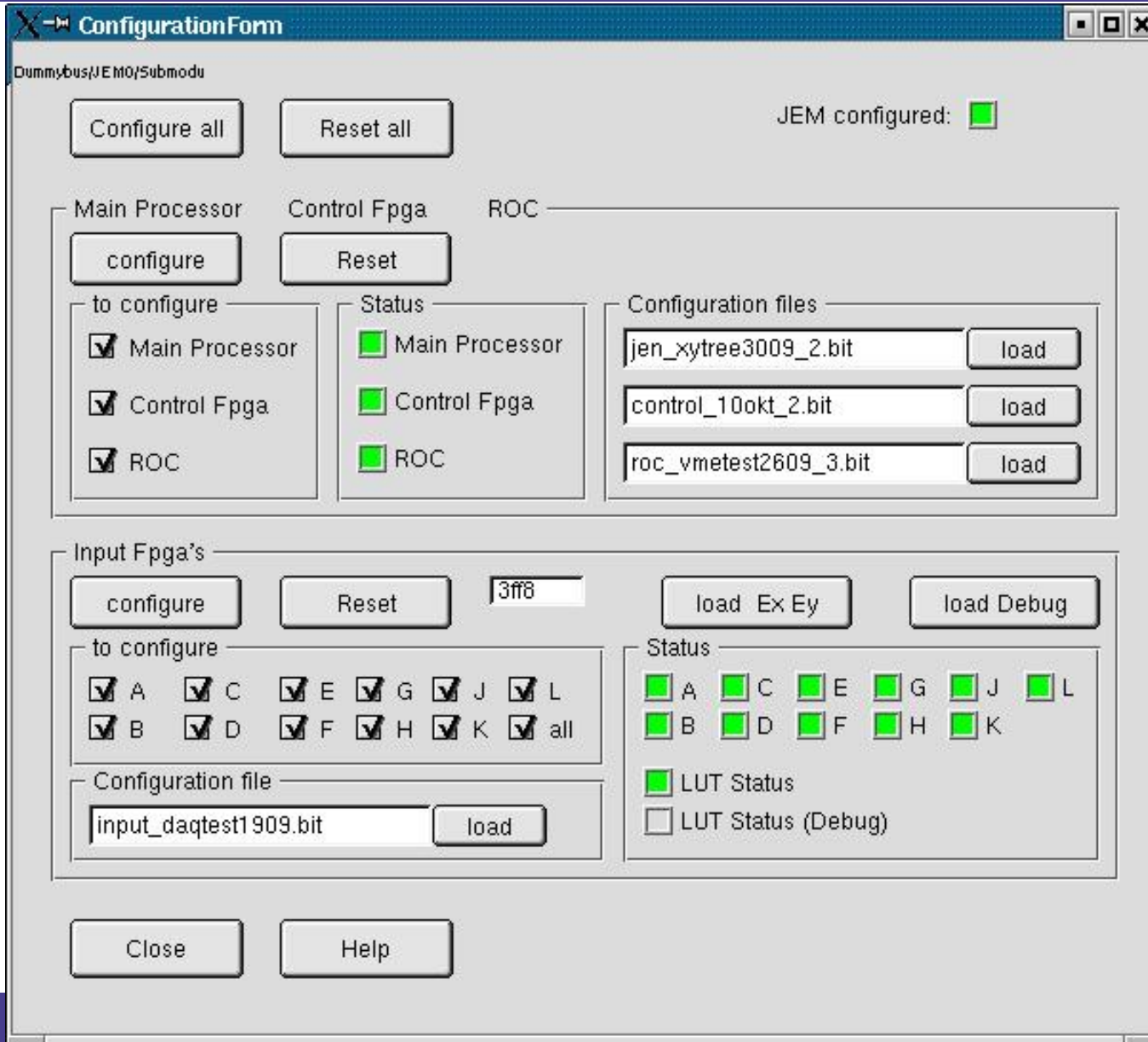




## NEXT STEPS

- Convert all existing software packages to HDMC and module services
- Next step: Integrate lookup tables, Link status, parity errors
- Then: Test vectors
- Expected to be finished end of November
- If possible we would like to work together for a couple of days in November with UK software people.

# SOFTWARE MODULES (HDMC)



Cano Ay, new  
PhD student:  
LUT included

# Status

Difficult to DEBUG HARDWARE and to WRITE SOFTWARE at the same time.

Good news: PhD student who can work most of his time on software development

# SUBSLICE TEST

- CPU from Mainz
- Online software if possible in HDMC/module services format
- Otherwise use existing shell script software

All new software will be written in HDMC/module services framework.