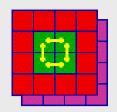


ATLAS Level-1 Calorimeter Trigger



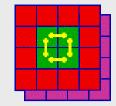
CP/JEP Rod Prototype Tests

"From the lone Sheiling of the misty island..."

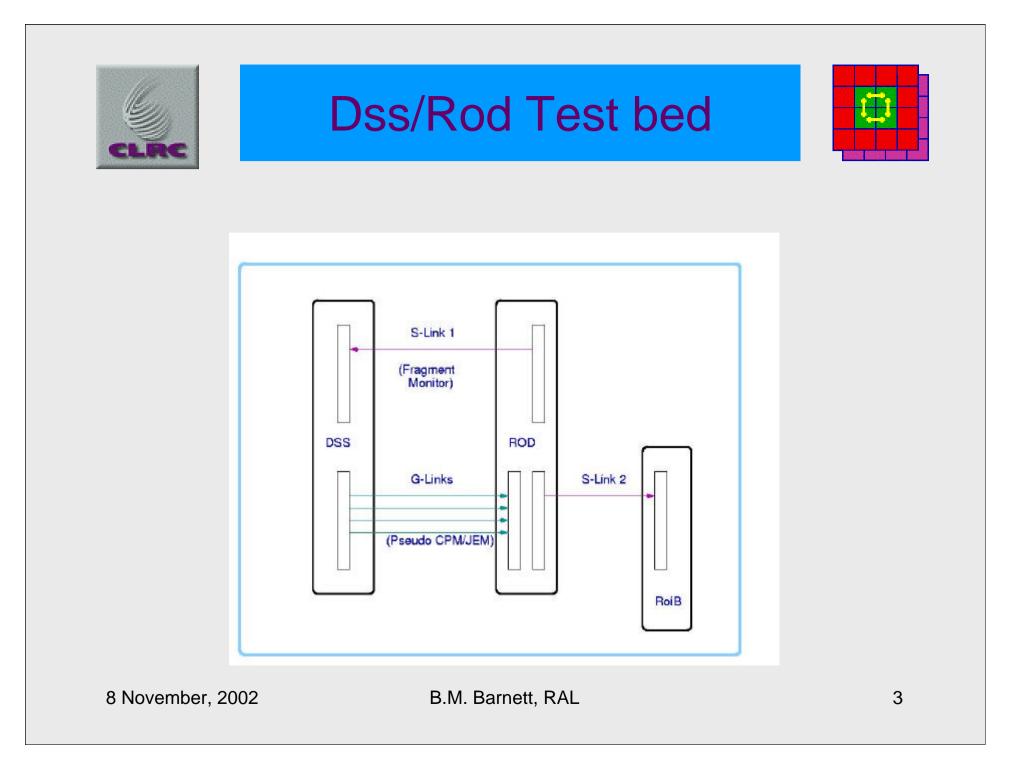
Bruce M. Barnett



Overview

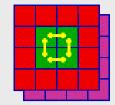


- Dss/Rod Test Bed
- Slink Think
- And Other Things
- Tutorials from Friends
- Integrated Looper
- Plans





Slink Think



Flow control issues resolved:

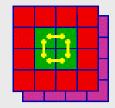
 "I disabled the comparator that tells me when a packet is finished when I suspend data transmission due to the LFF. If this happens when there is one word to go, due to a latency of 1 cycle, the comparator is still disabled... Regards James"

OusSignal -1ff_2 -slink_ful1_2 overflow_ettor_	* 1 1	0	15	26	27														
slink_bull_2		1	-		10	28	29	30	31	32	33	34	35	38	37	38	39	40	41
and the second particular second	1														8				- 3
overflow_error_		1		100				811	0.000						1		1	1074	
	0	0								_									
underflow_error	0	0																	
-wen_3	0	0																	
-en	0	0																()	
-wen_s_int	0	0																	
	0	0			1.00				1						1011	1	1000	1011	
uttel	1	1							1										
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and the second								0633				-							
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				003		(002)	00	11	Xaar	Y IEF	X 1FE	(1FD)	(1FC)	1FB)	1FA.)		1F	8	
<u> </u>		1112	<u>ย</u>			1	-		_		-	_	_		California (-		-	2
						18	Xt IO		-	गम	erle	-	4	10	(X-0)	10			
	- en - ven_s_int - uren - urtr1 - m_bof_rof T9_rd_count_inc H addra_2 H addra_2 H count int	-en 0 -ven_s_int 0 -uven 0 -utt1 1 -sn_bof_sof 0 19_r6_count_inc 0 8 addrs_2 005 8 addrs_2 003 9 count int 003 4 2 1	-en 0 0 -wen_s_int 0 0 -wen 0 0 -	-en 0 0 -wen_s_int 0 0 -wen 0 0 -	-en 0 0 0 -wen_s_int 0 0 -wen 0 0	-en 0 0 0 -wen_s_int 0 0 0 -wen_s_int 0 0 0 -wen 0 0 0 -ustal 1 1 1 -m_bof_sof 0 0 T9_r6_count_inc 0 0 0 H addra_2 0C6 0CF(0E0)(0E0) H addrb_2 0C3 0C3 0DC(0DD)(0DE) H count int 0031003 DB3 A P a a x x A	en 0 0 wen_s_int 0 0 uuten 0 0 uutel 1 1 em_bof_mof 0 0 19_cd_count_inc 0 0 # addra_2 005 005 005 005(005)(005)(005)(005)(005)	-en 0 0 0 Wen_\$_int 0 0 urtr1 1 1 1 en_bof_mof 0 0 19_td_count_inc 0 0 # addta_2 005005000(000)(000)(000)(000)(000) # count_int 003003 003 X002 X 00 X 0 X:0	en 0 0 Wen_s_int 0 0 usen 0 0 ustil 1 1 en_bot_sof 0 0 19_c6_count_inc 0 0 0	exit 0 0 Wen_s_int 0 0 usen 0 0 ustil 1 1 em_bof_mof 0 0 19_cd_count_inc 0 0 # addica_2 005 005 005(005)(005)(005)(005)(005)(000)(000	-es 0 0 0 -wen_s_int 0 0 0 -wen_s_int 0 0 0 -wen 0 0 -wen 0 0 0 -wen 0 0 0 -wen 0 0	-ea 0 0 0	-en 0 0 Wen_s_int 0 0 urte1 1 1 =s_bef_sof 0 0 19_m6_count_inc 0 0 # selet_sof 0 0 # selet_inc 0 0 # selet_inc 0 0 # selet_inc 0 0 # seleting 0 0 # seleting 0 0	-en 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	en 0 0 Wen_s_int 0 0 urte1 1 1 urte1 1 1 urte1 1 1 "B_ed_count_ine 0 0 B_edetca_2 0C6 0C6 0DF(0E0) 00-1000 B_edetca_2 0C3 0C3 0DC(0DD)(0DE)(0CF) 0E0 (0.002)(0E3)(0E4)(0E5)(0E5) B_edetca_2 0C3 0C3 0DC(0DD)(0DE)(0CF) 0E0 (0.002)(0E3)(0E4)(0E5)(0E5) B_edetca_2 0C3 0C3 0DC(0DD)(0DE)(0CF)(0E0) (0.001)(000^{ont})(1EF)(1FE)(1FE)(1FC)(1FE)) B_edetca_2 0C3 0C3 0D3 (002)(001)(000^{ont})(1EF)(1FE)(1FE)(1FE)(1FE)(1FE)(1FE)(1FE	-ea 0 0 Wen_s_ist 0 0 usen 0 0 ustil 1 1 ==s_bot_sof 0 0 13p_td_count_ist 0 0 # seleta 2 005 005 005 (000) (00	exa 0 0 Wen_s_sint 0 0 usen 0 0 usts1 1 1 es_bef_sof 0 0 19_sd_count_ine 0 0 9 addrs_2 005 005 005(000)(005)(005)(005)(005)(005	-ea 0 0 Wen_s_int 0 0 urte1 1 1 -m_bot_sof 0 0 13_Ed_count_inc 0 0 Wedta_2 000000000000000000000000000000000000	-ea 0 0 Wen_\$_sist 0 0 usen 0 0 usts1 1 1 ==s_bot_sot 0 0 19_sd_count_inc 0 0 #=s_bot_sot 0 0 #=sdot_sot 0 0 #=stat 0 0 #=stat 0 0 # > 0 # > 0 # > 0 # > 0 # 0

8 November, 2002



And other things



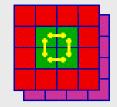
- Transient problems:

- Rod Sometimes enters a 'funny' state ...
 - » eg, after power glitch.
 - » glink problems....sometimes not all channels work on powerup.
- **CP-Slice-16**: Bit 23 set in hit data words. (awaiting test)
- CP-Slice-17: Incorrect Treatment of PP->CPM status Bits (S-ink trailer and hit words). (to be discussed.)
- Design complements:
 - The S-Link FIFO condition "EMPTY" should be indicated by (a) status bit(s). (We have link-full to date...)
 - Zero suppression should be applied to the hit words

B.M. Barnett, RAL



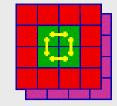
Tutorials from friends



- Tutorial from James.
 - Very clear, instructive. Illustrated well some of the complexities of his design.
 - But after a morning, we had only scraped the surface.
 - Serialiser/Cp-Chip sessions possible.
- Impressed with hdl_designer
 - also a very good documentation tool.
 - Access to code and a read-only version (or read-only access, by covenant) will help us understand/ document.

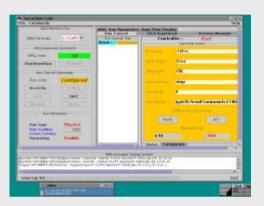


Integrated Looper



7

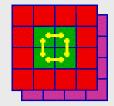
- Looper
 - started life as a stand alone code to drive the testbed.



- Looper functionality is now integrated with l1calo daq environment and is the usual Rod test tool:
 - run control accesses moduleServices to prepare modules
 - kicker drives dss frame generation, reads out and compares
 - integrated hdmc provides interaction/display in parallel.
- integrated with online db, provides statistics to IS server (with M.L. help) and MRS (potentially fatal errors.), as well as the runcontrol and simulation (thanks gurus!)
 8 November, 2002
 B.M. Barnett, RAL

CLRC

Plans



• What Next?

- Check zero suppress (slice) still ok. (CP).
- Confirm Rol firmware still ok. (CP)
- Other firmware variants ready (cmm, jem)
 - Software (l1calo) capable of handling it!
 - Simulation now available (Thanks, Steve!)
 - So just to get on to it...
- Other Rod Modules:
 - Thanks to Adam ... Checked for
 - » mechanical completeness, basic++ functionality.
 - » Ready to be vector processed!

8 November, 2002

B.M. Barnett, RAL