Pre-Processor ASIC

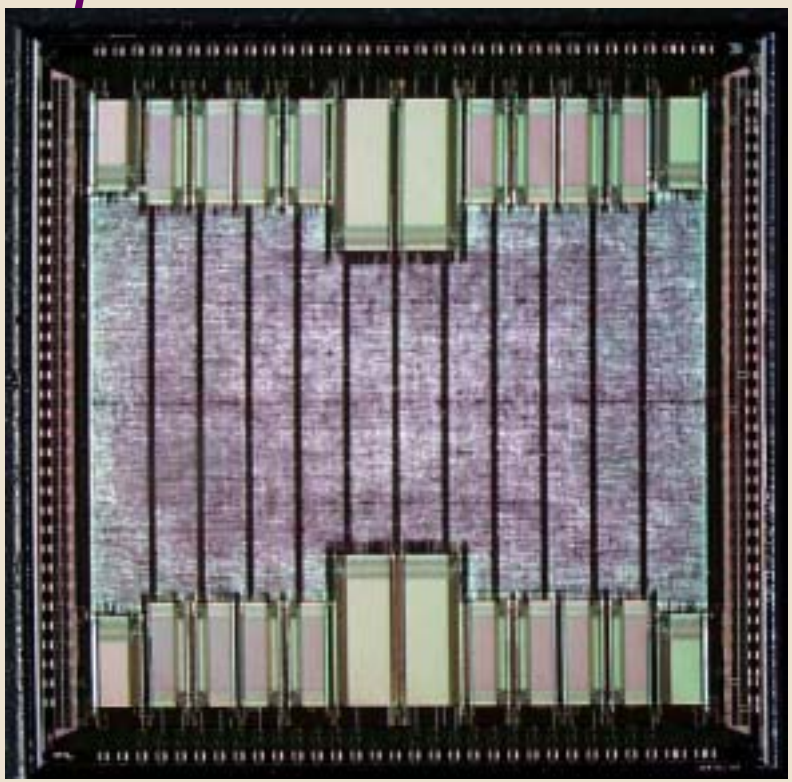
submitted: 04/25 - January - 2002

shipment: 12 - March - 2002

to be delivered: 3-4 wafers, 1 diced into individual chips

out-line

- ☞ *Design parameters*
- ☞ *A flash-back on Pre-submission status*
- ☞ *Power-up defaults*
- ☞ *Documentation*
- ☞ *on-chip logo*



Design parameters

AMS-CUP 0.6µ CMOS process
3 metal (Aluminium), 2 Poly layers

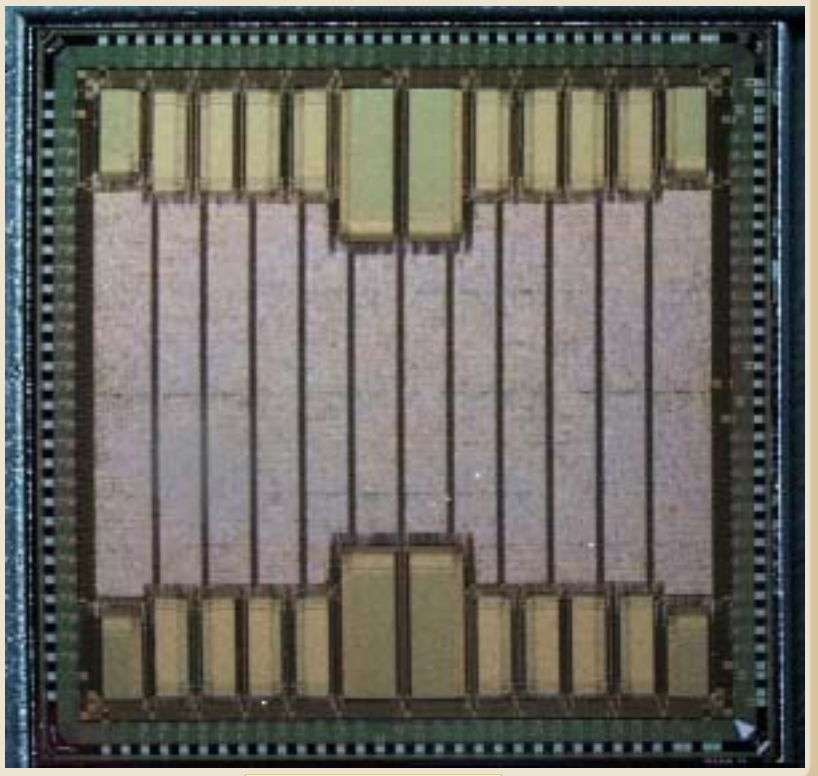
999k Transistors, 41k Standard Cells, 8.125 kbyte RAM

137 pads: 1 temperature, 32 power, 5 JTAG, ...

Voltage : 3.3 V

At estimated 40% Toggle rate

Power / current consumption: 2.5W / 700 mA



Flash-Back

Pre-submission timing analysis/simulation

- τ *Static timing analysis on the netlist + sdf-back annotation*
  - *Revealed timing problems on paths to/from RAM blocks, on paths crossing clock domain boundaries / gated clocks*
- τ *Timing simulations on the entire chip + sdf timing information*
  - *Revealed timing violations (RAM, clock tree, RESET, ...) some functional errors/inconsistencies (next slide)*
- ⏭ *required modifications in Verilog code, synthesis and layout! Several iterations were done to find the optimum combination*
- τ *Automatic test generator not able to produce test vectors*
  - *Hence, only functional tests possible*

Flash-Back

Pre-submission changes/modifications

- τ *Asynchronous RESET problems at RAM control blocks*
  - *Internally synchronized RESET to all RAM's*
- τ *Wrong parity generation on the 2nd half BC-MUX*
  - *Fixed to generate odd-parity*
- τ *BCID decision bits 1 clock tick later than BCID result*
  - *Corrected by removing extra logic!*
- τ *Sat-BCID result sometimes 1 clock tick late (fixed delay)*
  - *Due to signal shape and digital thresholds*
    - *delay made programmable (new register)*
- τ *Latching of ADC signals on clock negative-edge critical*
  - *Due to relatively short time for arithmetic*
    - *At least one level of pipelining is necessary*

Power-up defaults

Some real-time path related settings

- *ADC / Ext-BCID latched on Clock neg-edge*
- *One pipeline level on ADC / Ext-BCID*
- *LUT by-passed (8 MSB of the ADC put on output)*
- *FIR-filter coefficients: 0, 0, 1, 0, 0*
- *SAT-BCID digital thresholds/saturation: 255, 767 / 1023*
- *ET-range boundaries: 0 : 511 : 895 : 1023*
- *Decision logic: peak-finder, ...+Ext-BCID, ...+SAT-BCID*

Documentation

Status

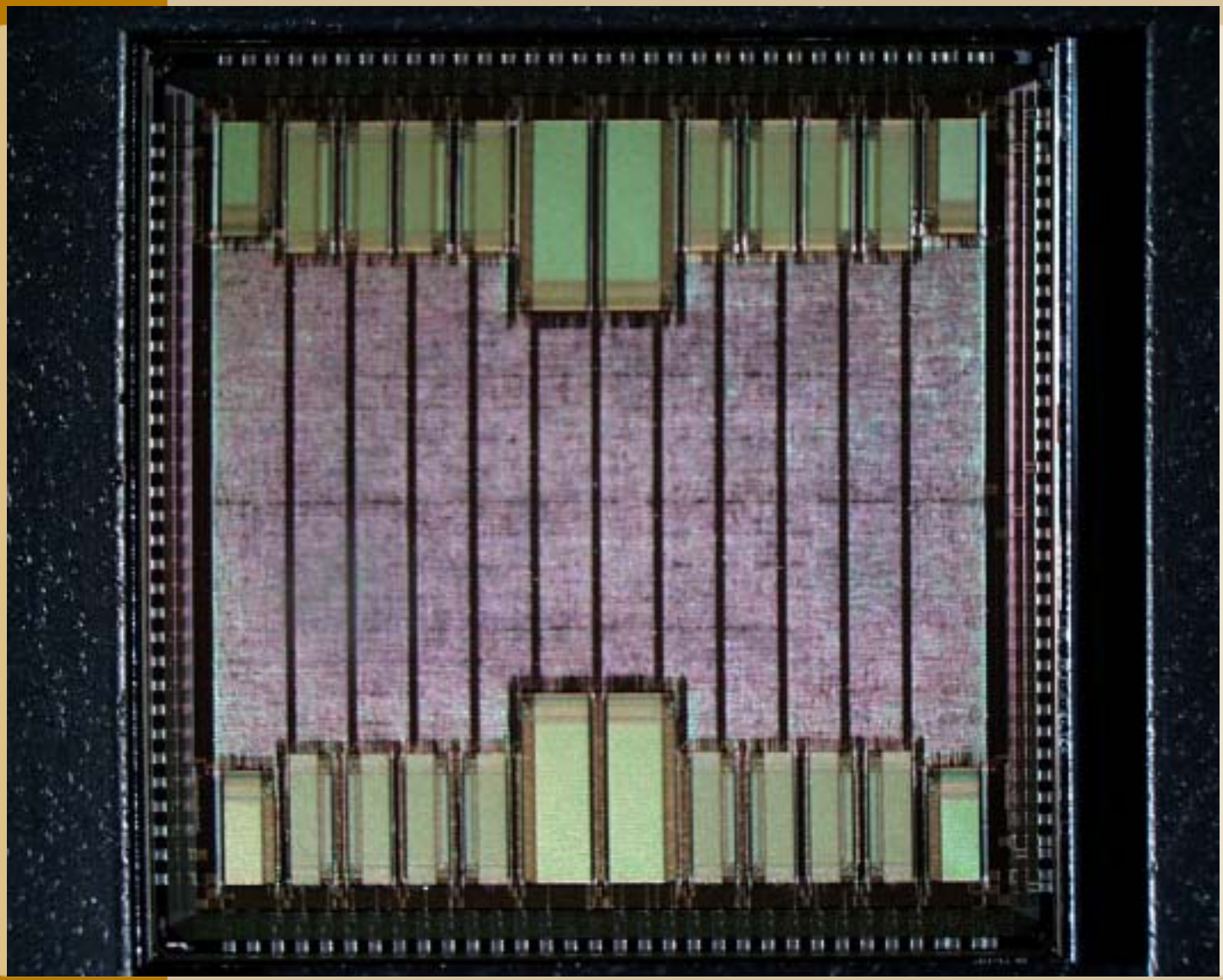
- *Verilog code / synthesis scripts / layout macros in CVS*
- *Several Test-bench/test-vector modules in CVS*
- *Generated database/netlist/layout files archived*
- *Design-guide documentation almost complete (layout done)*
- *Manual needs more work - done in a month or so!*
  - *When done, CVS-repository will be tagged as release 1*

on-chip ATLAS logo

This ATLAS logo is etched on the lower right corner of the chip

List of Chip Designers

ASIC Die



ATLAS LOGO