Common Merger Module

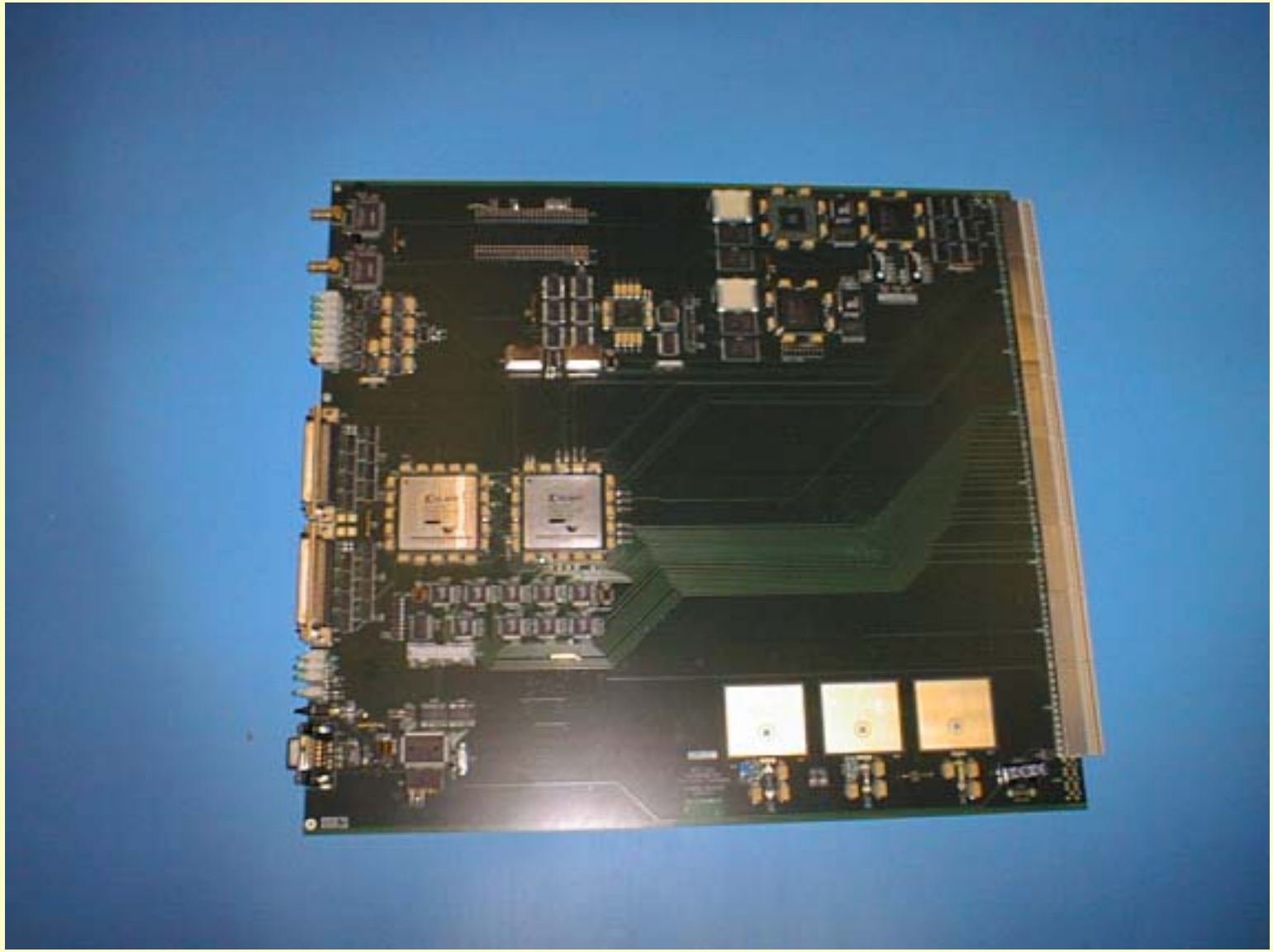
(and associated modules/test cards)

Status and Test Plans

CMM Status

- Five boards manufactured - one assembled
- Design problem picked up just too late:
  - Two JTAG chains connected together via Flash RAM controller CPLD
  - Impossible to separate - tracking on buried layer would need to be cut
- Temporary solution - remove “offending” CPLD
- Consequence - Crate Merging FPGA cannot be configured *via* Flash RAM
  - However, it can be configured *via* its JTAG chain
  - Board power-down/up will require re-configuration via external JTAG connection
- JTAG testing starting ~now - needs Crate/PB for module power+cooling
- Ensure all CPLDs and FPGAs can be configured correctly
- Finally, VME checkout → release to Physics Group for sub-system Tests

CMM – an existence proof!



CMM-related Modules

- *For complete sub-system tests, new hardware is needed:*
- **General-purpose I/O (GIO) Cards to source emulated HIT data** *(CMC card driven from DSS module)*
  - **STATUS: designed, awaiting layout**
- **CPM Emulator (CPME) Cards in CPM slots to inject HIT data into PB** *(driven from GIO)*
  - **STATUS: in manufacture**
- **General-purpose I/O (GIO) Card to sink merged HIT data from CMM** *(together with DSS, emulates CTP-D)*
  - **STATUS: designed, awaiting layout**
- **Rear Transition Modules (RTM) to link Crate and System CMMs**
  - **STATUS: designed, awaiting measurement of crate mechanics before finalising layout**

Ideas for CMM Test Procedures

- ***Six stages of testing:***

- **First two stages will be in Electronics Test Lab**

1. **Module "health checks" *(mechanical, power, etc)***
2. **Bench tests (*JTAG, VME--, FPGA configuration, CAN, … using LabView)***

- **Final four stages will be in Physics Group Lab**

3. **Check readout of Slice data into ROD**
4. **Check real-time Crate-level merging with emulated HIT data**
5. **Check real-time System-level merging operation**
6. **Check real-time true data-flow operation at full System-level**

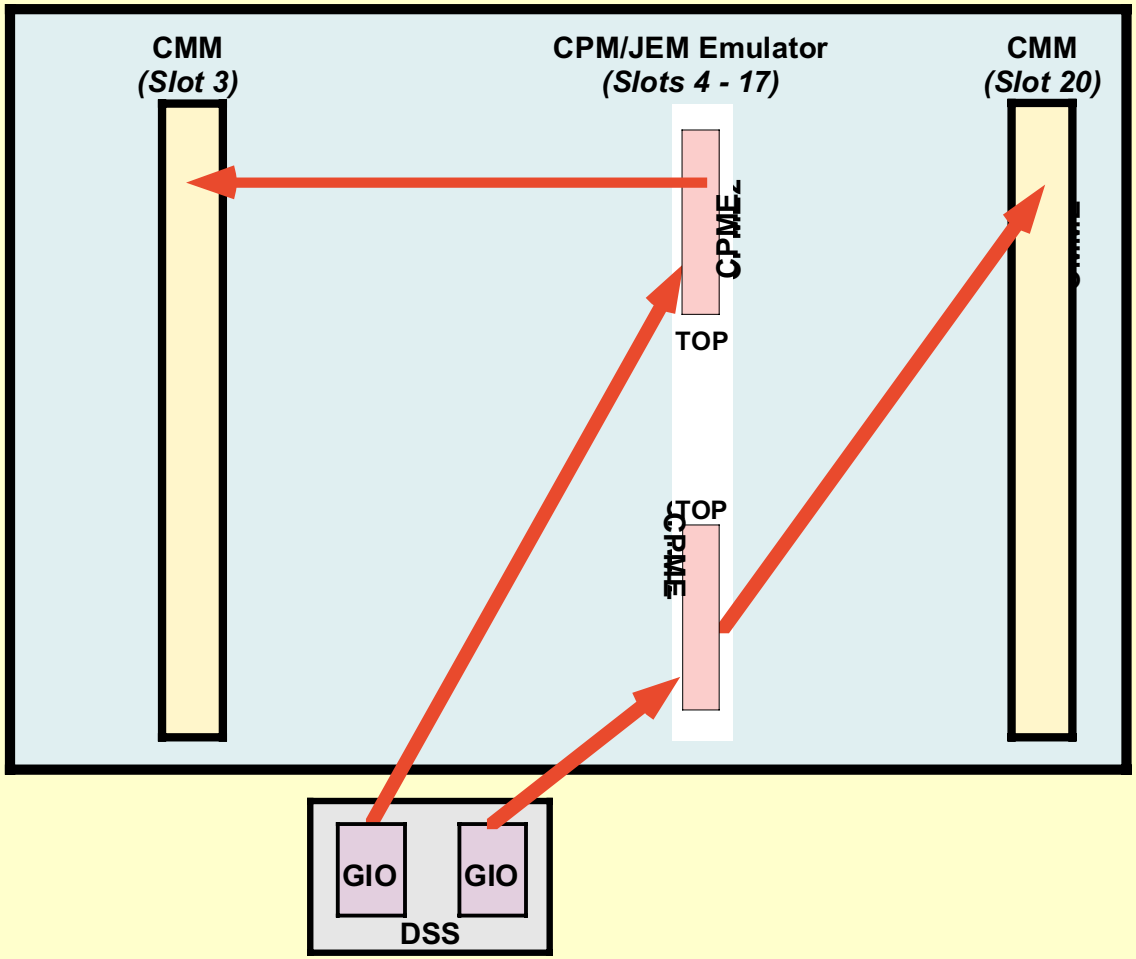
- **Large amount of hardware + firmware + software needed from ~Day 1**

Stage 3 - Readout functionality

- ***Read-out of pre-loaded Slice data into ROD:***
- **Requires TCM, TTCdec, D-ROD**
- **Set up TTC system - TCM + TTCdec on CMM**
- **Load test data pattern - e.g. ramp - into scrolling input memories via VME, channel by channel**
- **In Playback mode, propagate these data patterns through the merging algorithms into scrolling output memory**
- **Stop clocks and read output memory via VME**
- **Repeat tests with L1A transferring Slice data into D-ROD at up to 100KHz *(needs appropriate firmware)***
- **Explore timing margins**

Stage 4 - Real-time functionality (1)

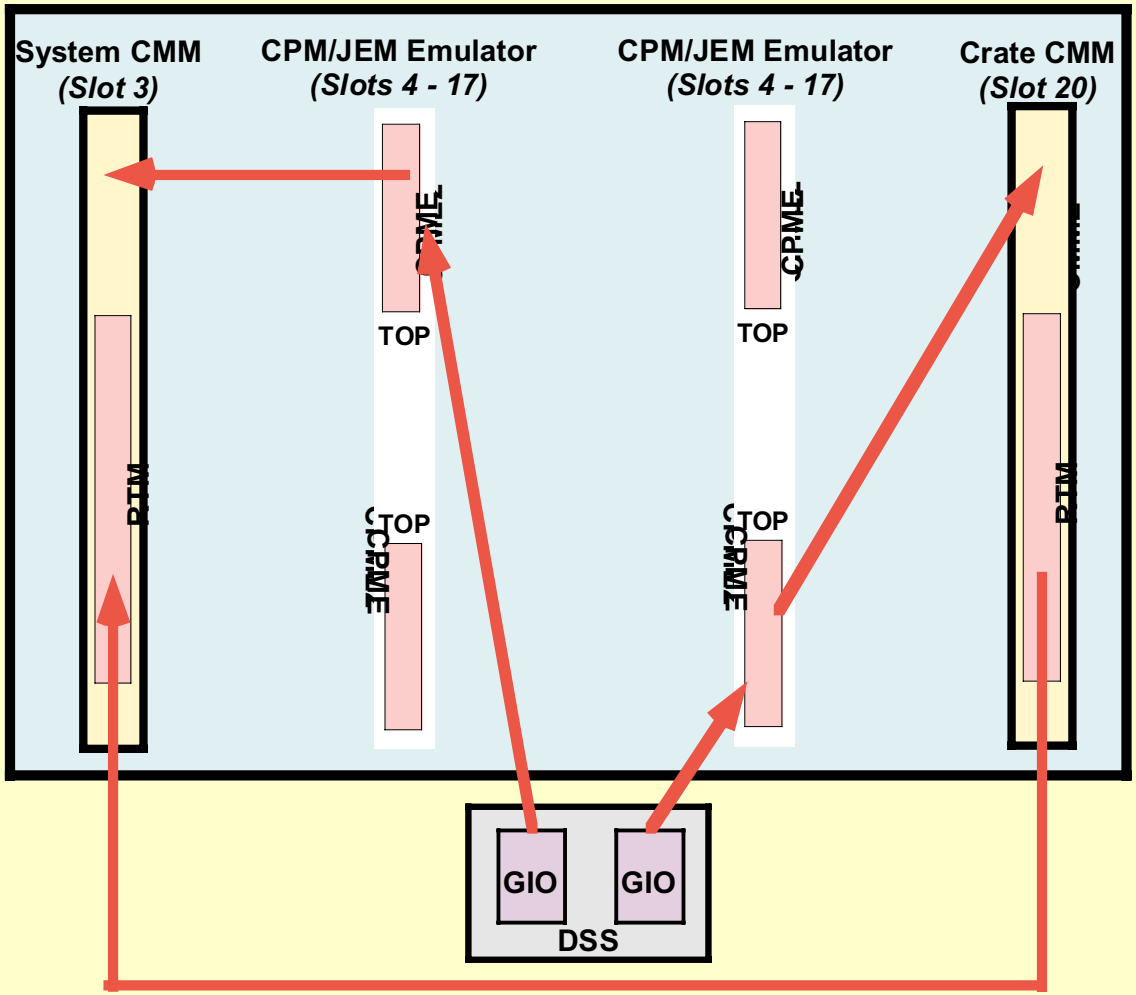
Crate-level merging using real-time emulated CPM HIT data:



- *Requires CMM, TCM, TTCdec, D-ROD, CPME, DSS, GIO*
- Load DSS with data patterns *(ramps, etc)*
- With CPME in each CPM slot in turn, clock data into CMM via PB
- Stop clocks, read input memories via VME, check correct data capture
- Tune timing as needed
- Repeat with L1A triggers at up to 100KHz and read out ROD data
- Verify correct algorithm performance

Stage 5 - Real-time functionality (2)

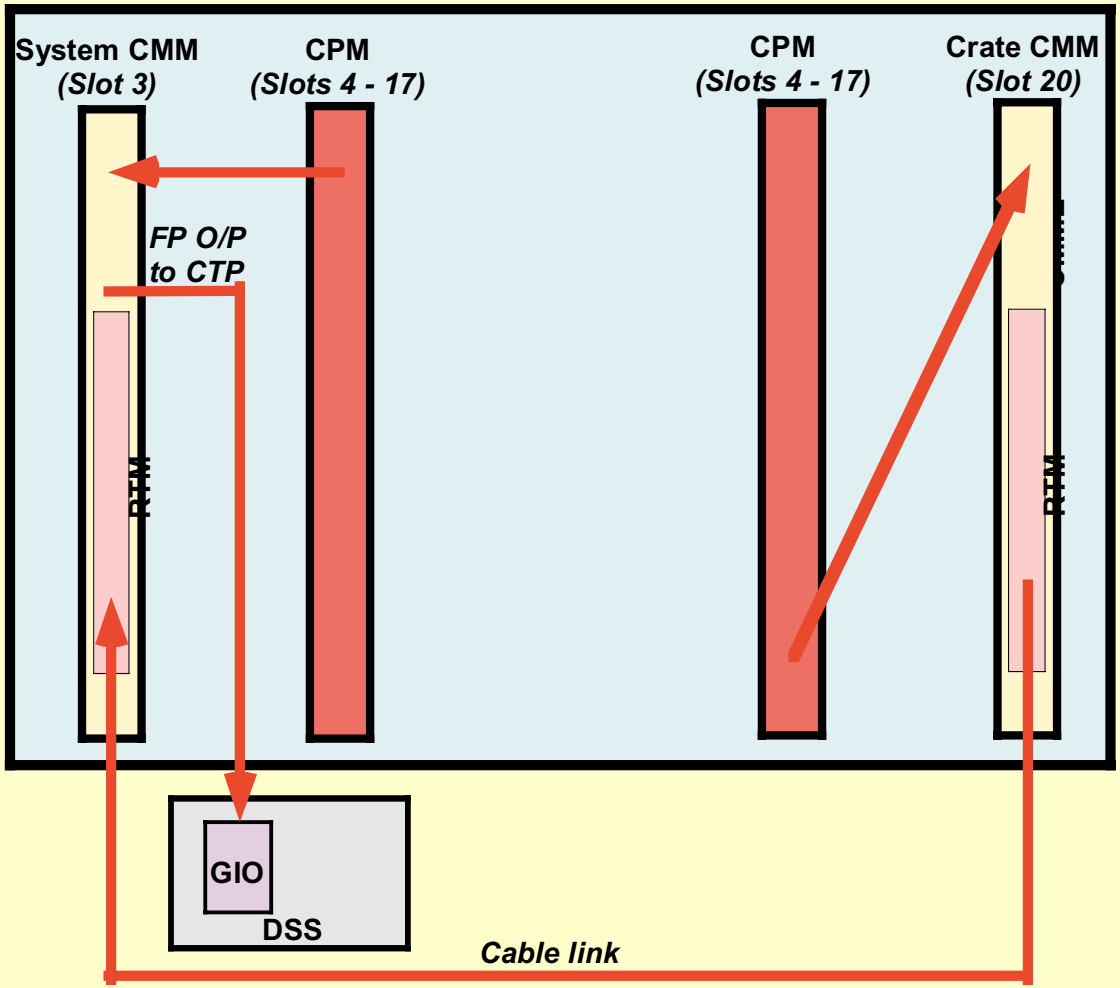
System-level merging using real-time emulated CPM HIT data:



- *Requires CMM, TCM, TTCdec, D-ROD, CPME, DSS, GIO, RTM*
- Load DSS with data patterns *(ramps, etc)*
- CPMEs in 2 CPM slots, clock data to Crate and System CMMs via PB
- Stop clocks, read System CMM input memories via VME, check correct data capture
- Adjust System CMM pipeline delay as needed to merge data correctly
- Repeat with L1A triggers at up to 100KHz and read out D-ROD data
- Verify correct algorithm performance

Stage 6 - Real-time functionality (3)

System-level merging using real-time true CPM HIT data:



- *Requires CMM,TCM, TTCdec, D-ROD, DSS, GIO, RTM, CPM*
- **Load CPMs with data patterns *(ramps, etc)***
- **With CPMs in 2 CPM slots, clock data into Crate and System CMMs via PB**
- **Stop clocks, read Crate and System CMM input memories via VME, check correct data capture**
- **Read out DSS and verify correct CTP data**
- **Repeat with L1A triggers at up to 100KHz and read out D-ROD data**
- **Verify correct algorithm performance**

CMM Test Programme

- **Conclusions:**
  - **This will be a lengthy test programme!**
  - **Some hardware is still not finished - CPME, RTM, GIO, ...**
  - **With the CPM test programme running in parallel, we are confined to a single Crate/Backplane assembly**
  - **A lot of new firmware is needed - for RODs *(Slice and RoI)* and for CMMs *(for JEP)***
  - **We will need to build a team of hardware, firmware and software people**