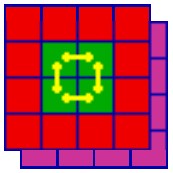


Highlights and Dunkel-lights: Heidelberg, 14–16 March 2002

- Personal view, not a comprehensive summary of all that was presented and discussed.
- Apologies for anything important that's missed — tell me.
- If you think anything is mistaken or objectionable please say so!

- Categories are as follows:

  \+ A positive, or mainly positive, development, or something that has been sorted out, or simply good progress.

  – A negative development, or something that needs to be sorted out that may cause problems, or an item where work seems to have stopped — no criticism of people involved is (necessarily) implied.

  ◆ More work or a decision is needed.

  ! A controversial point that must be discussed further.

- No names mentioned since it's very difficult to be fair to everyone who has done all the work — people will know who they are!

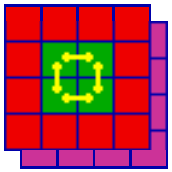
Physics simulation

+ **Work continues to progress on trigger simulation**
+ **Jet trigger almost done, energy triggers soon**

– **Problems with documentation of CMT add to existing problems in using ATHENA**

- **Must finish E_T algorithms**
- **Must add features such as thresholds varying with location**
- **Must decide how to simulate grey areas such as noise added en route to the trigger, and who will do that**

+ **New B-physics work on using RoIs from calorimeter trigger to guide LVL2 for muon triggers — saves on LVL2 resources needed**



Calorimeter signals and cables

+ Gain of TileCal summing amplifiers now looks o.k. in view of energy lost in dead material

+ Rack layout situation now seems more or less sorted out

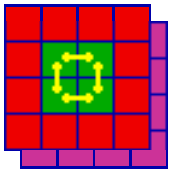
– Who builds receivers (TileCal and even LAr) still not formally defined, but we will know about LAr and maybe even TileCal soon (also said this last time)

– TileCal cable situation has not progressed

◆ Must fully document connections from calorimeters to Preprocessor (also said this last time)

◆ Must write specifications for TileCal receivers

◆ Need to liaise with calorimeter calibration people to make sure our requirements are known, and to aim for future integration tests (in beam?) — set up a working group to do this



Preprocessor

+ ASIC has come back from AMS
+ Many problems in design were found and fixed
+ Documentation updated

+ MCM design updated and detailed test plans shown, including use of video RAM

– Video RAM can't be synchronised to external clock, so most slice testing must start from digital data **(also said this last time)**

◆ MCM documentation still needs updating

+ Much work done on REM FPGA firmware (and documentation)
+ Compression now allows readout of 1 BCID + 3 raw data slices at full speed

– ROD delayed due to pressure of other work
– Software and simulation work delayed due to pressure of hardware and firmware work

! Still needs 2 S-links per ROD, but how do we define what is 'normal' readout for ≤100 kHz rate and what is 'diagnostic'? Not a sharp definition!

CPM and JEM

+ CP FPGA tests ok with GTM so CPM is now needed
+ CPM is about to start tests, following well-defined programme

+ JEM 0.1 about to be tested; so far it looks as if problems using fine-pitch BGAs on 9U boards are resolved
+ Work on JEM firmware under way

+ Nice work done on jet algorithm
+ New work on JEM simulation under way

– Some JEM components lack boundary-scan capability

◆ JEM documentation will need updating
◆ Test plan for JEP subsystem needs to take account of what is ready when at the PPM and CPM interfaces

! Desirable JEM FPGA upgrades raise question of whether to iterate design before building more modules for slice test

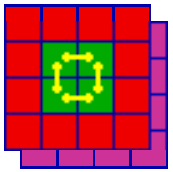
Common modules and backplane

+ CMM has arrived, test programme about to start
+ Backplane has arrived (and documentation finished)

+ TCM, adapter link card and VMM progressing well
+ Further progress on debugging CP/JEP ROD prototype

– Small error on CMM means PCBs must be re-made
– Infuriating problem of unavailability of pins for backplane

◆ Similar question to PPr for CP/JEP readout about what data rates we need to handle for normal running



DCS, CTP, etc.

+ CAN-4-USB allows CAN diagnostics from PC

+ Discussion on damaging FPGAs by loading wrong configuration is already producing ideas for building in additional safety

+ CTPd and patch panel being prepared for slice test
+ Design of final CTP is now multi-module, and hence much more flexible
+ Serious work on trigger menus and configurations
+ CTP simulation started; uses experience of calorimeter trigger offline simulation

– Still cannot get Fujitsu to accept CAN frames

◆ Try to find out what Fujitsu problem is
◆ Better choices for on-board chips seem to exist, closest to what we want seems to be new Hitachi

! Although having a microcontroller per module seems like overkill, the cost and overhead are low, and it allows us to decide later how elaborate a monitoring system to use

◆ Do as much as possible locally, to minimise data flow to SCADA system

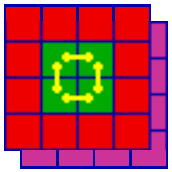
Online software

+ Much progress on module services, databases, simulation (documented!), individual modules, Linux systems ...
+ Steps made towards setting up test runs, including use of databases
+ Document summarising data formats in progress
+ ROD-crate DAQ at last getting needed attention!

– Could get close to required schedule if we could take all people writing software and isolate them from the world for ~2 months! But of course we can't!
– It would help if ROBin/ROS solutions stopped proliferating

! Still very short of effort to develop software, so try to see what software and tests might be de-scoped and/or deferred; re-assess objectives

! Try to get non-software experts to do as much module testing as possible (also said this last two times)



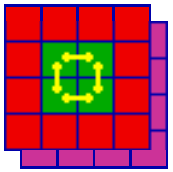
Slice test and timescales

+ **Modules and ASICs are now starting to appear!**

– **Individual and subsystem test phases will be complex and it is very difficult to predict duration (also said this last two times)**

– **Slice test now in Autumn, was Spring at last meeting!**

◆ **Must not send modules for slice test until they are working well on their own *and* in their own subsystem (also said this last time)**



Summary

+ **People are being very open about problems as well as successes**

+ **There has been a great deal of progress, and now a lot of hardware is starting to exist. Very exciting period is just starting!**

– **... But also more slips in timescale, and shortage of effort (also said this last time)**

Thank you to the Heidelberg group for a productive, well-organised meeting in lovely surroundings!

Best wishes for your lovely new building!