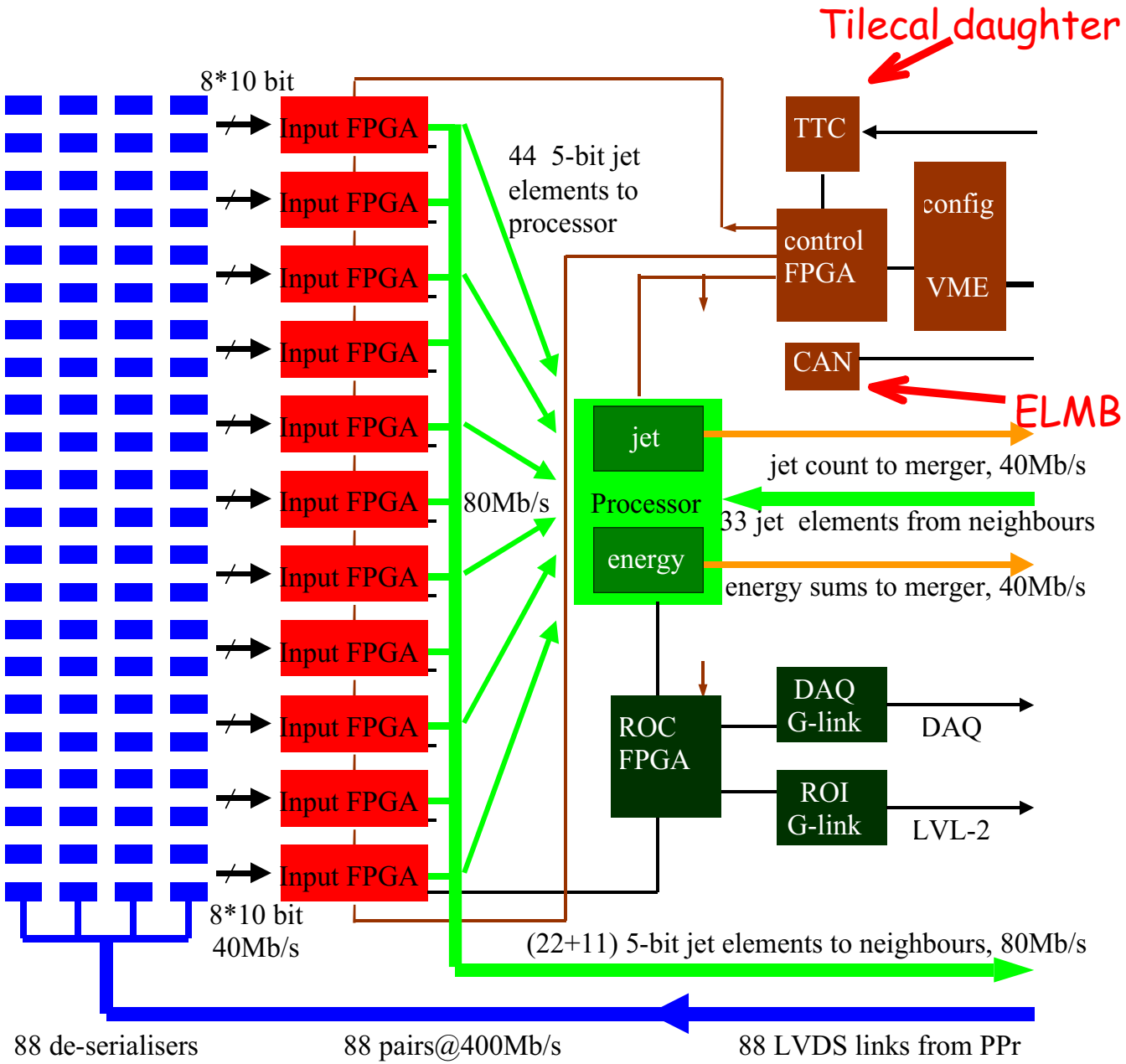
JEM0 (*)

- JEM0 Hardware : overview, history, and status
- JEM0 Firmware : algorithms, status
- JEM – plans and timescale

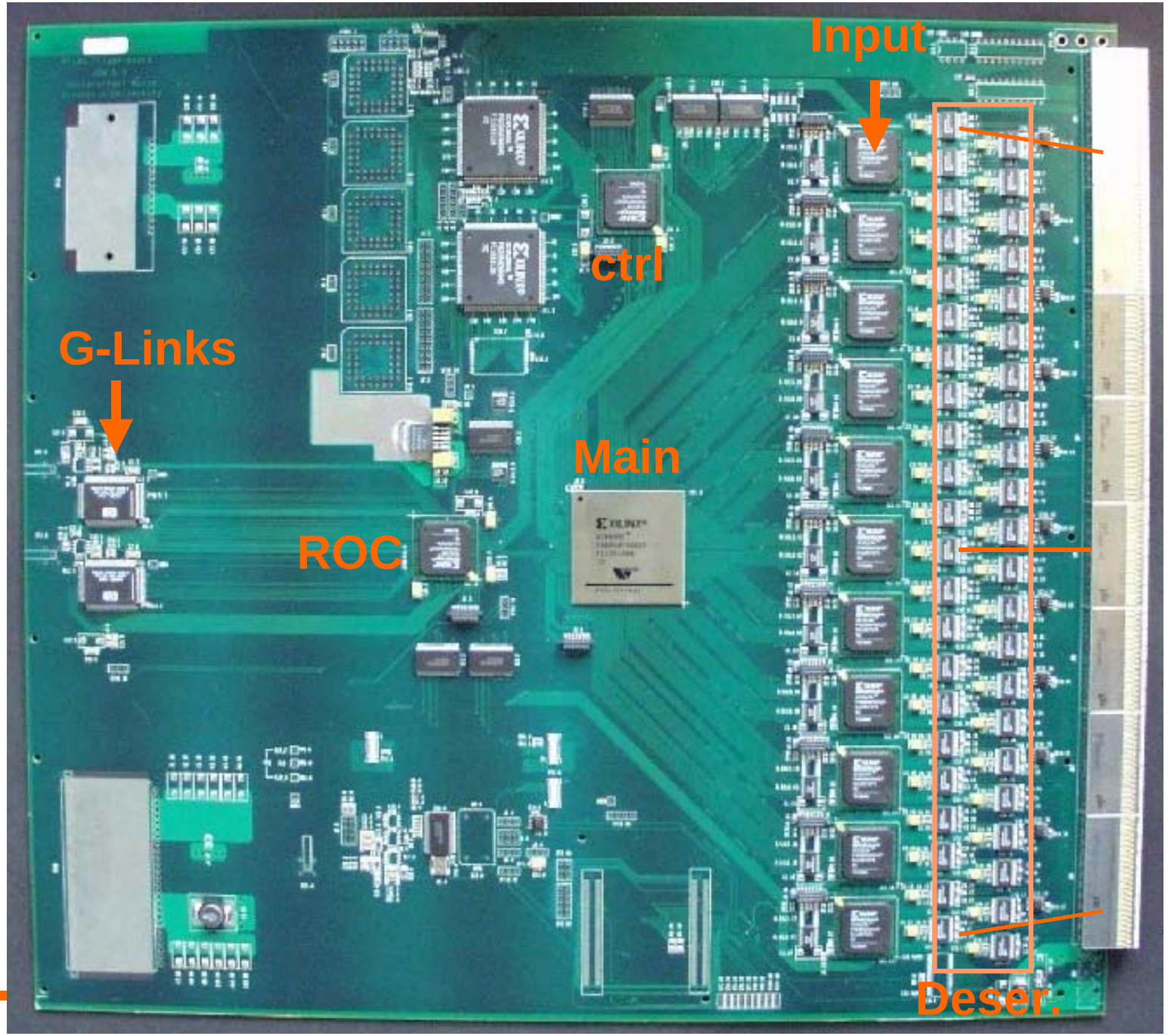
(*) Module0 specifications : last update draft 0.8d (Nov.13, 2001)

http://www.physik.uni-mainz.de/schaefer/browsable/JemSpecsFinal

JEM
-Block Diagram-



JEM0.0
-top view-



the JEM0 production saga

02.01.2001 board design files to PCB manufacturer (Andus)

- PCB production fails, 2nd run required
- module 0.0 assembly (Mair) utter failure, re-work required
- XC2S150 fail (non-documented power-down) -> re-work again

-- Nov. 2001 : joint meeting (RAL) --

05.11.2001 order a new PCB (module 0.1) from Andus
22.11.2001 PCB delivered. Electrical test & impedance test (at Andus) : ok.
01.12.2001 module 0.0 back from re-work. Looks ugly. Requires re-rework in our lab. Backplane connectors still not well aligned.
14.11.2001 send module 0.1 to Rohde & Schwarz for assembly & test.
16.01.2002 module 0.1 back from assembly (X-rayed at R&S : ok). Module looks good. No obvious connectivity problems.

-- 2 months assembly time include 1 month waiting for tantalums to arrive –

Both modules powering up successful. Starting first tests…

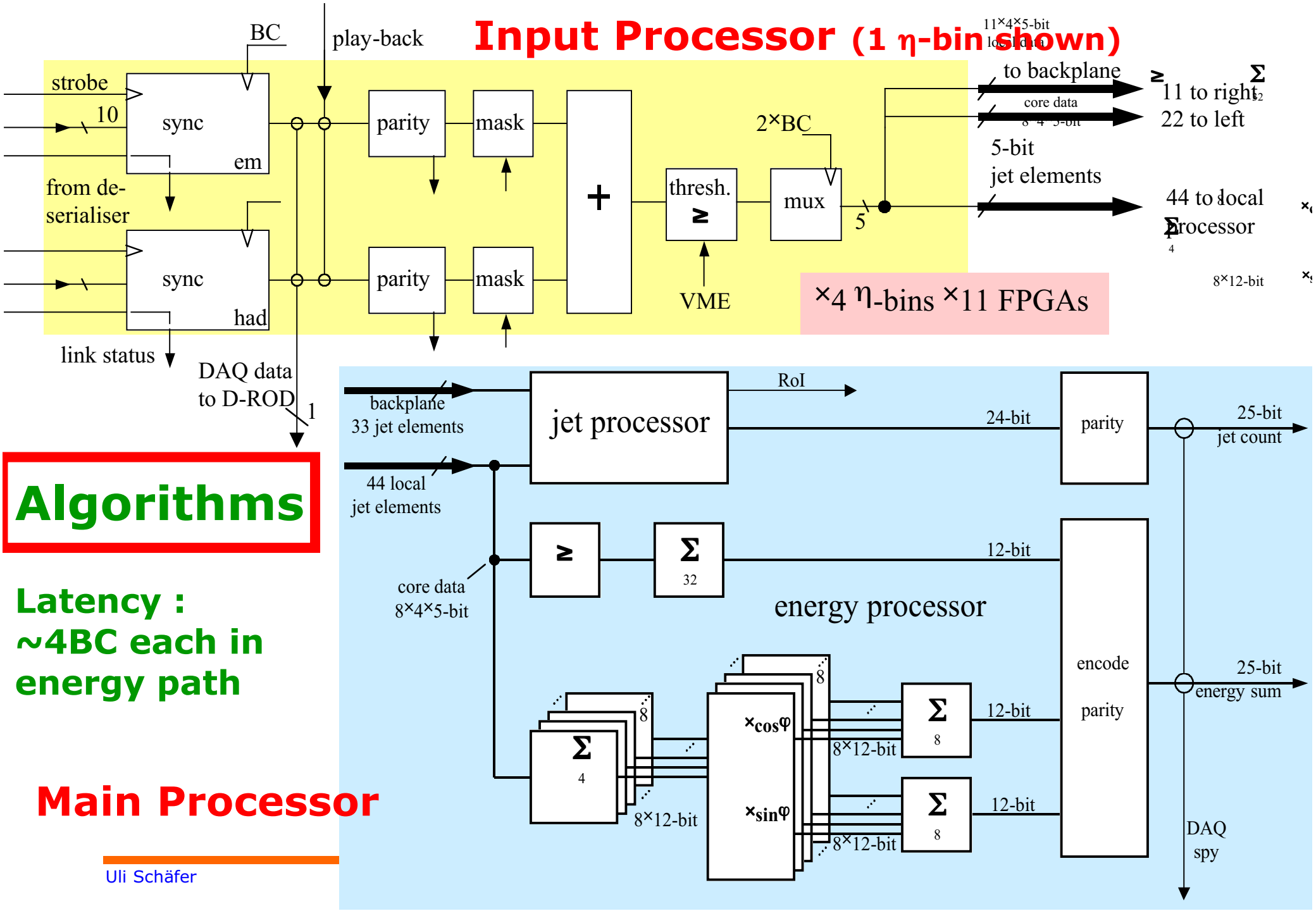
the JEM0 hardware status

The current module was designed to **module0 specifications**. Therefore it is considered a fully functional module with full channel count. Some **implementation details** are considered non-final and should be revised before start of mass production, if possible.

Known issues:	resolve :
TTC interface missing (availability of daughter bd.)	before slice test
DCS interface missing/non-final	before and after
Very scarce logic resources on main processor	before or/and after
Logic resources on input FPGAs	after slice test

And at lower priority:

Improvement of B/Scanability (de-serialisers, ...)	?
Coherence of TTCrx control (HW?)	?
Coherence of DCS sub-system	?
Coherence of FPGA configuration mechanisms (HW?)	?
Simplification of VME access	?


Input Processor (1 η-bin shown)
BC
play-back
strobe
10
sync
em
from de-serialiser
sync
had
link status
DAQ data to D-ROD
1
parity
mask
parity
mask
+
thresh.
≥
VME
2×BC
mux
5
to backplane
core data
11 to right
22 to left
5-bit jet elements
44 to local processor
×4 η-bins ×11 FPGAs
Algorithms
Latency : ~4BC each in energy path
Main Processor
backplane 33 jet elements
44 local jet elements
core data 8×4×5-bit
jet processor
RoI
24-bit
parity
25-bit jet count
≥
Σ 32
12-bit
energy processor
Σ 4
8
8×12-bit
×cosφ
×sinφ
8×12-bit
Σ 8
12-bit
Σ 8
12-bit
encode
parity
25-bit energy sum
DAQ spy

Uli Schäfer

Firmware Status

- VME CPLD carries a basic VME interface including FPGA-configuration download port
- Input FPGA almost finished. Input synchronisation derived from the CP code at an early stage, might require update.
- Main processor: Top level and energy processor almost finished. Need to instantiate jet processor. FCAL handling will have to be modified due to revised allocation of FCAL channels.
- Control FPGA lacks TTC interface
- ROC code still incomplete, Andrea working on that.
- Modifications to VME control path (see next slide)

JEM0 test status Hard-/Firmware

JEM0.0: No systematic connectivity tests after last re-work.
use module (as is) as a test-bed for firmware (Andrea)
Problems discovered with VME access. Timing ?
→ Convert all FPGA control code (main processor, ROC) to fully synchronous, using I/O flip-flops
→ Convert input FPGA control code (RDO ring bus !) to synchronous where possible.
Prepare HW (DSS) and SW for test of real-time data path (Thomas)

JEM0.1: Try to systematically test connectivity, using JTAG/BS (Bruno)
Test equipment: JTAG Technologies PM3705 Explorer + VIP automatic test generation.
requires endless exception lists due to large count of non-BS´able devices → avoid use of non-BS´able components in future designs, don't expect connectivity test results too soon!

Considerations for next iteration

JEM0.1 looks good (though connectivity test results are not yet available).

- Assembly of 9Ux40cm modules is nontrivial and expensive, but possible.
- We need to improve testability. JTAG/BS seems useful only if most of the components are B/scannable. Be careful with choice of components for next iteration. Fortunately scannable LVDS de-serialisers are available now.
- BGA re-work equipment is expensive and we might rather rely on services from the private sector.
- It is not yet clear whether there is any advantage of standard pitch vs. fine pitch components. Cheapest currently listed high-pin count (624 User-I/O), 1.28mm pitch BGA is XC2V2000-4BF957C at $860. That's ok for main processor. For input FPGAs etc. standard pitch (XC2V1000-4BG575) will cost an additional $126,000 total ! That's unacceptable.This means input processor daughterboards will be required if we want to rule out fine pitch BGAs on 9U Modules.

Plans / timescale

Slice test – summer 2002:

- JEM0.1 hardware ready to go into slice test unless connectivity problems found in ongoing tests
- ELMB and TTCrx daughter (to be built) need to be integrated
- A lot of work required on firmware and software
- After successful standalone tests, 2 further JEM0s need to be manufactured (possibly with larger main processor chips, XCV1000E). This will take ~ 1 month if all components are available and if the current economic situation persists

Future plans

- We need to decide on improvements on de-serialisers (JTAG/BS), processor FPGAs, and CAN. If overall timescale slips, we might decide to design a new module early on, so as to avoid major board revisions immediately before start of mass production.