Status of the RemFPGA

Dominique Kaiser

diploma student
KIP Heidelberg

Dominique.Kaiser@gmx.net
dkaiser@kip.uni-heidelberg.de

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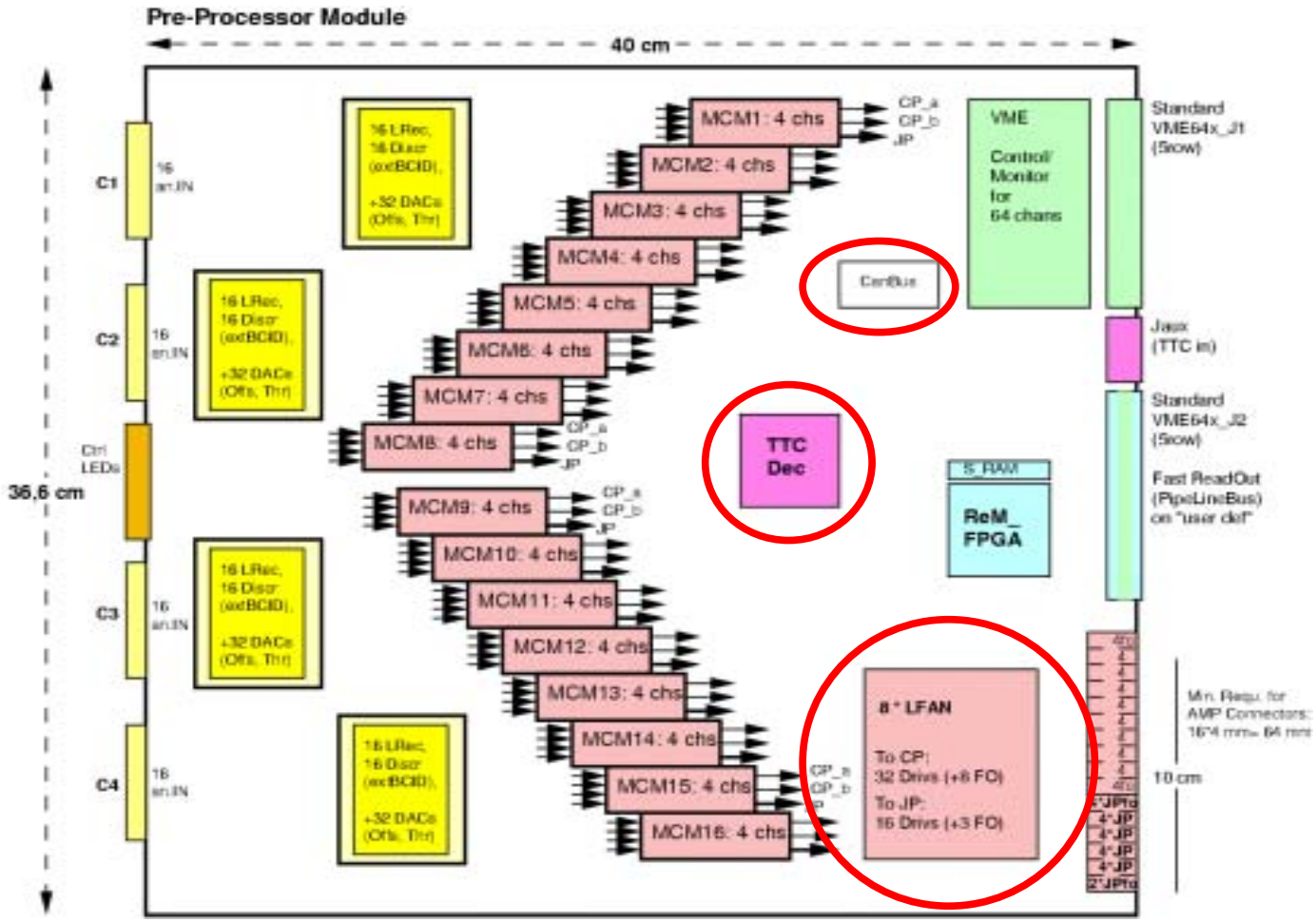
What am I talking about...



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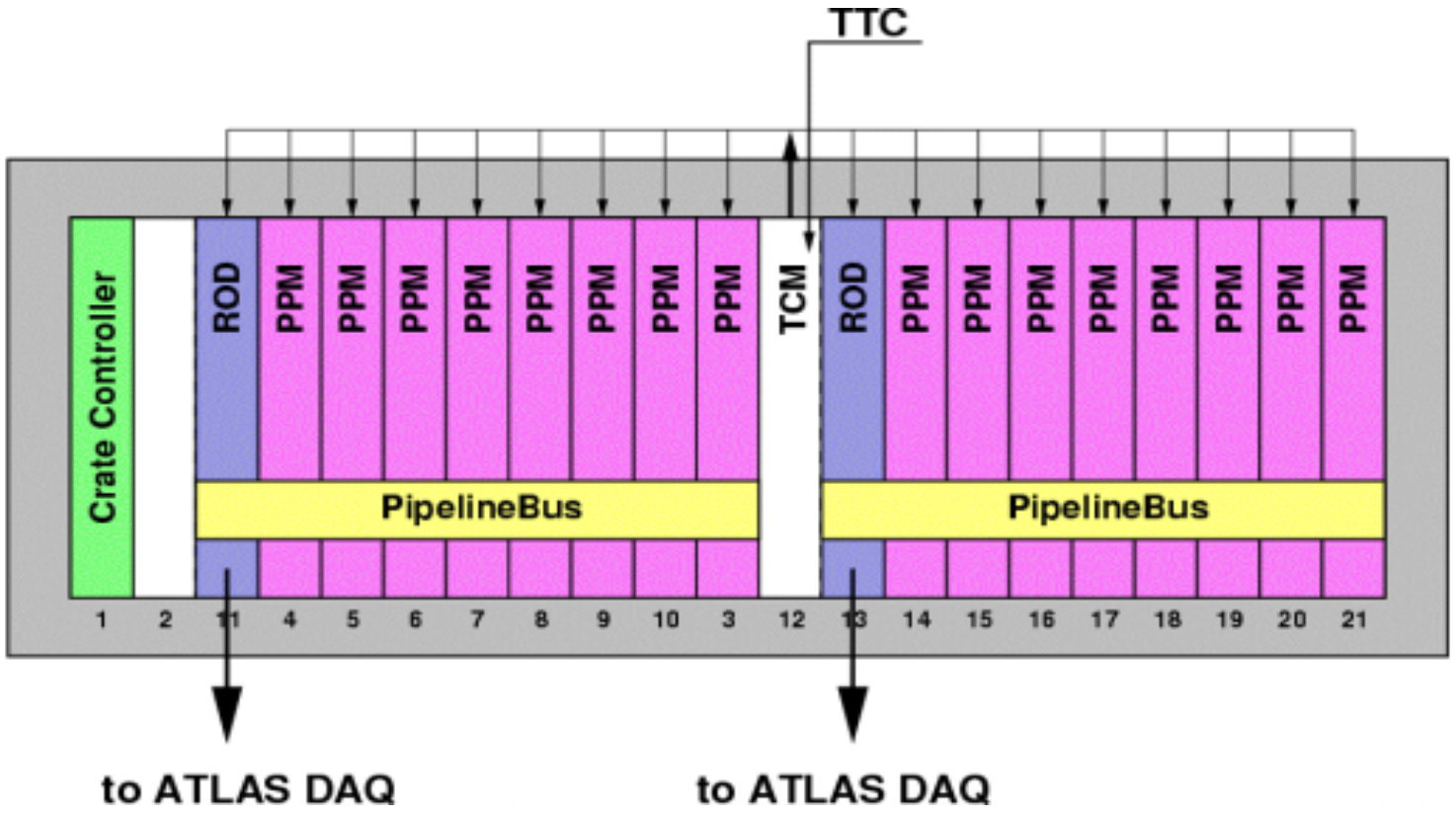

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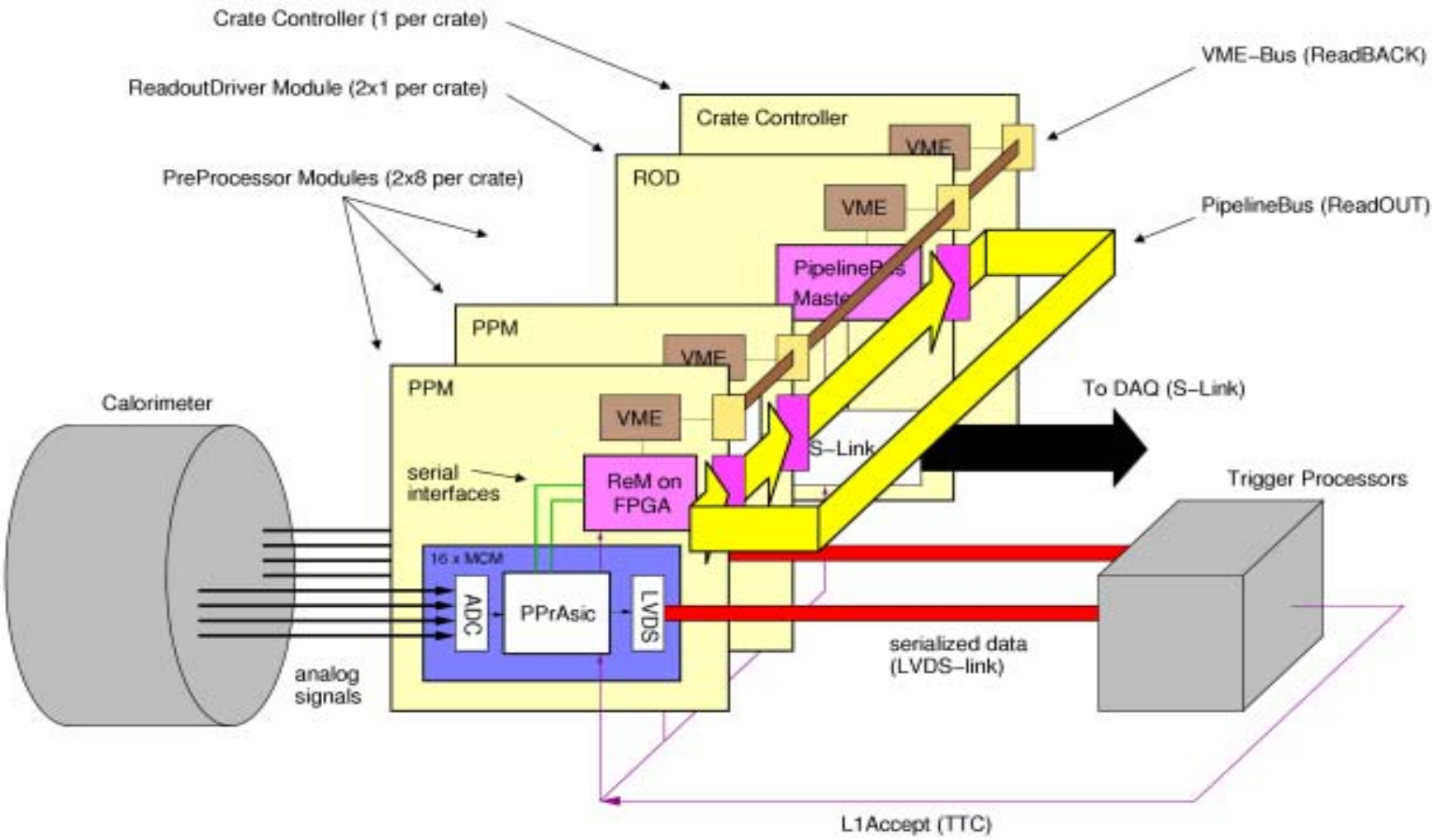


Interfaces of the RemFPGA

- 32 serial - 2 to each MCM / PPrASIC
- 1 I2C - connected to all 16 MCMs (Phos4 chip)
- 4 SPI - 1 to each Analog Input Board (4 MAX529 DACs on each)
- 1 VME - connected to VME CPLD ("easy VME" interface)
- 1 PLBus - connected to backplane

Serial interface

- Used for all PPrASIC configuration
- Used for PPrASIC ReadOUT
- Used for ReadBACK of Histogramms and Rate-meter information
- Custom 13Bit protocol
- Controled by RemFPGA
- 4 data lines (In, Out, Clk, Frame)
- All data lines are differential

I2C interface

- Used only to configure Phos4 on MCMs
- 2 data lines (SDA, SCL)
- Data is only written to Phos4, not read
- Slow I2C bus speed – 100kbps
- Used I2C VHDL-code from OpenCore.org
- Controlled by RemFPGA (I2C master)

SPI interface

- Used only to configure DACs on AnIn
- 3 data lines (Data, Clk, CS)
- Very simple serial shift protocol
  (multiple devices are daisy-chained)
- Data is only written, not read
- Controlled by RemFPGA (data source)

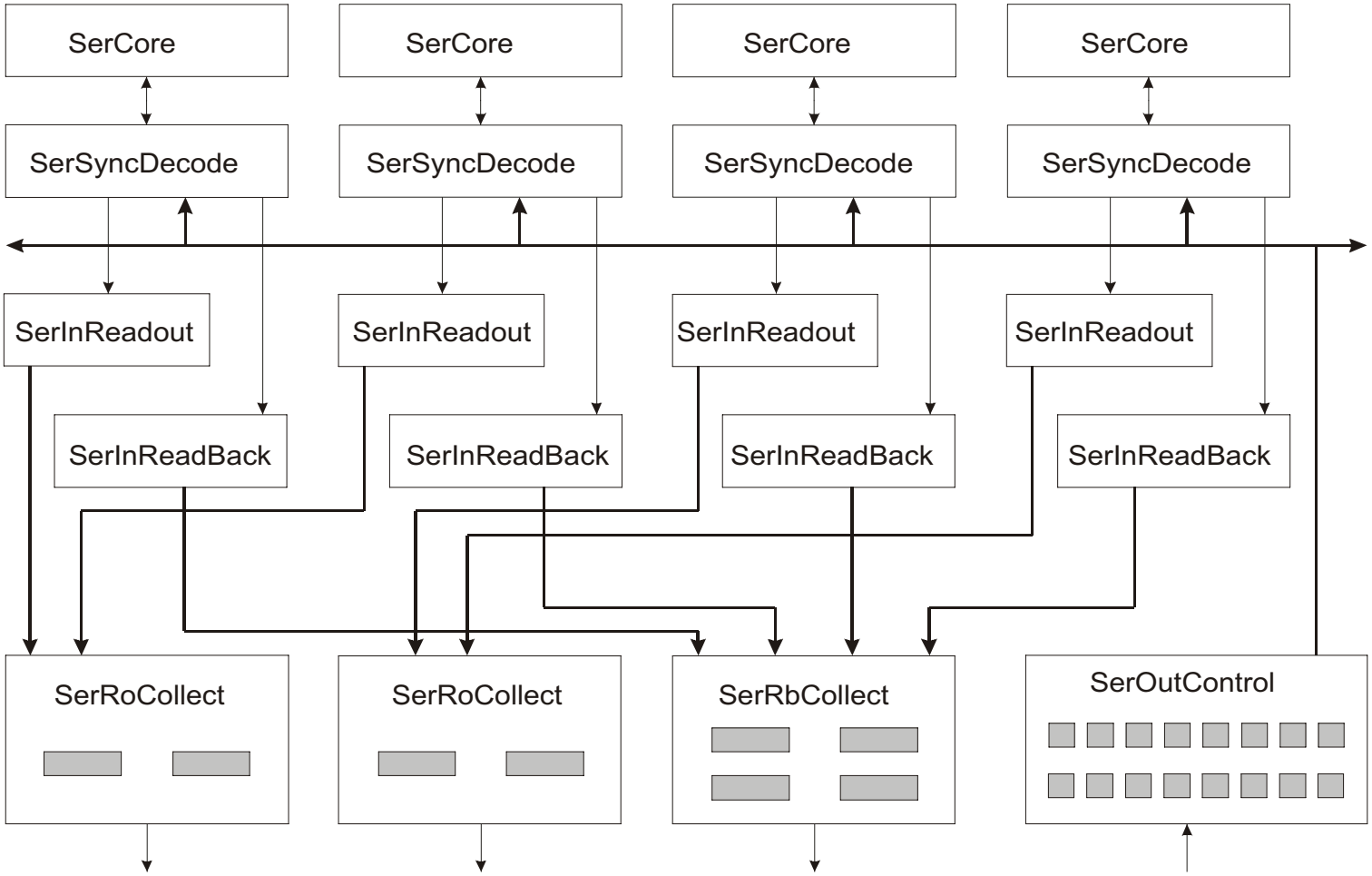
“easy VME” interface

- No real VME bus interface at all
- Connected to VME CPLD
- 60 data lines (32Data, 22Address, Sel1, Sel2, DS, RW, RDY, Interrupt)
- Can access all RemFPGA interfaces
- Can access RemFPGA registers directly
- For data input/output a FIFO scheme is used (i.e. no memory address scheme)

PipelineBus interface

- Connected via backplane to the previous and next module in the crate
- 72 data lines (34Data, Parity, Clk)
- Can access all RemFPGA interfaces and internal registers
- Controlled by ROD (RemFPGA is slave)
- 60MHz clock -> 240 MB/s

Details of serial interfaces



PipelineBus interface

- Intended for PPrASIC ReadOUT data
- Data bandwidth of 240 MB/s just fast enough for ReadOUT, but nothing else
- Use PipelineBus for ReadOUT only
- Use VME for config and status analysis
- Use VME for Histogramm and Rate-meter

VME Interface

- VME and PipelineBus offer the same commands and functionality
- Too slow for ReadOUT data of 8 PPMs
- Fast enough for ReadOUT data of 1 PPM
- Much easier to access registers via VME than via PipelineBUS
- Interrupt available

Bandwidth and compression

- 100kHz (75kHz) L1-Accept rate
- 1 BCID sample per channel (8+3 Bits)
- 5 (3) RAW samples per channel (10+1)
- Flag bits per channel (5 – 13 Bits)
- Flag bits per PPM (8 - 16 Bits)
- PipelineBus commands and idle cycles

Bandwidth and compression

Data type	Bits	Multiplier	Total Bits	Compress	MB/s	MB/s
BCID Sample	8	512	4096	2	48.83	24.41
BCID Algorithm	3	512	1536	1	18.31	18.31
RAW Sample	50	512	25600	2.2	305.18	138.72
RAW Ext BCID	5	512	2560	1	30.52	30.52
Flags (per channel)	1	512	512	1	6.1	6.1
Flags (per PPM)	18	8	144	1	1.72	1.72
PBus (per PPM)	32	8	256	1	3.05	3.05
PBus (per ROD)	384	1	384	1	4.58	4.58
Data rate: 100 kHz			**35088**	**1.84**	**418.28**	**227.41**

- **100 kHz L1-accept rate**
  - (1:5) - 227.41 MB/s
  - (1:3) - 171.92 MB/s
  - (1:0) - 58.17 MB/s
- **75 kHz L1-accept rate**
  - (1:5) - 170.56 MB/s
  - (1:3) - 128.94 MB/s
  - (1:0) - 43.63 MB/s

Changes since RAL meeting

- **100 kHz L1-accept rate**
  - (1:5) - 227.41 MB/s
  - (1:3) - 171.92 MB/s
  - (1:0) - 58.17 MB/s
- **75 kHz L1-accept rate**
  - (1:5) - 170.56 MB/s
  - (1:3) - 128.94 MB/s
  - (1:0) - 43.63 MB/s
- **100 kHz L1-accept rate**
  - (1:5) - 275.38 MB/s
  - (1:3) - 207.68 MB/s
  - (1:0) - 106.14 MB/s
- **75 kHz L1-accept rate**
  - (1:5) - 206.53 MB/s
  - (1:3) - 155.76 MB/s
  - (1:0) - 79.61 MB/s

Bandwidth and compression Consequences

- PipelineBus
  - 40MHz _ 160MB/s
  - **60MHz _ 240MB/s**
  - 80MHz _ 320MB/s
- ROD
  - Data rate doubled _ FPGA speed issues ?
- S-LINKs
  - Two double-rate links needed (2x 128MB/s)
  - Consequences for DAQ (storage, speed, etc.) ?

State of RemFPGA verilog code

- Serial interface - done
- I2C interface - done
- SPI interface - done
- PipelineBus - done
- VME Interface - nearly
- Compression & error check - done
- Control logic, registers, etc. - done
- Testing of code - nearly

Conclusions

- 1 BCID : 5 RAW now possible at L1-rate of 100kHz
- RemFPGA is basically done
- Place and Route done
- Back-anno. timing analysis done
- FPGA Resources (Virtex 1000E)
  - approx. 40% of CLBs
  - approx. 90% of internal SelectRAM (88 of 96)
- Now hard at work writing the documentation
- To be done (by someone else): ROD FPGA code

Questions & Answers