Kirchhoff-Institut
für Physik

ATLAS Level-1 Calorimeter Trigger

Joint Meeting @ Heidelberg, Mar.2002

Universität
Heidelberg

Pre-Processor (System Issues)

- *The PPModule*
- *PPM "daughters": AnIn, LVDS, DCS, TTCdec*
- *TCM adapter*
- *Software for PPr-Hardware*
- *Schedule, "System" docs*

Paul HANKE, KIP Heidelberg

The PPModule

- *Schematics*
  - *- "almost" complete*
  - *- Power to the "component" population:*
    +2.5V ; +1.8V, +5.0 CleanVolt, -5.0 CleanVolt are needed
    (+5V, +3.3V are there from crate with ample Amps)

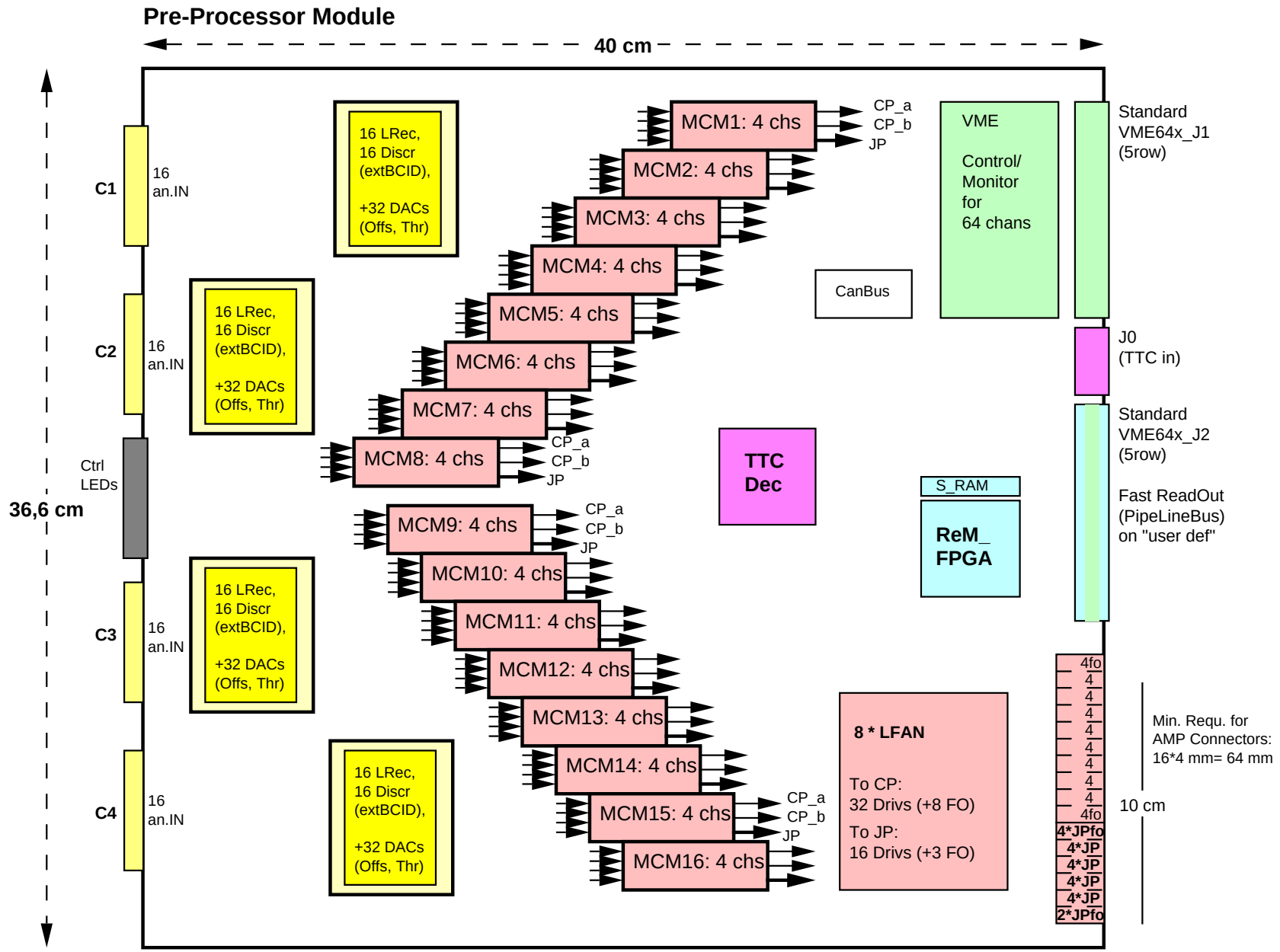
- *FloorPlan*
  - *- PPM is basically a "carrier" board (except for Rem_FPGA ...)*

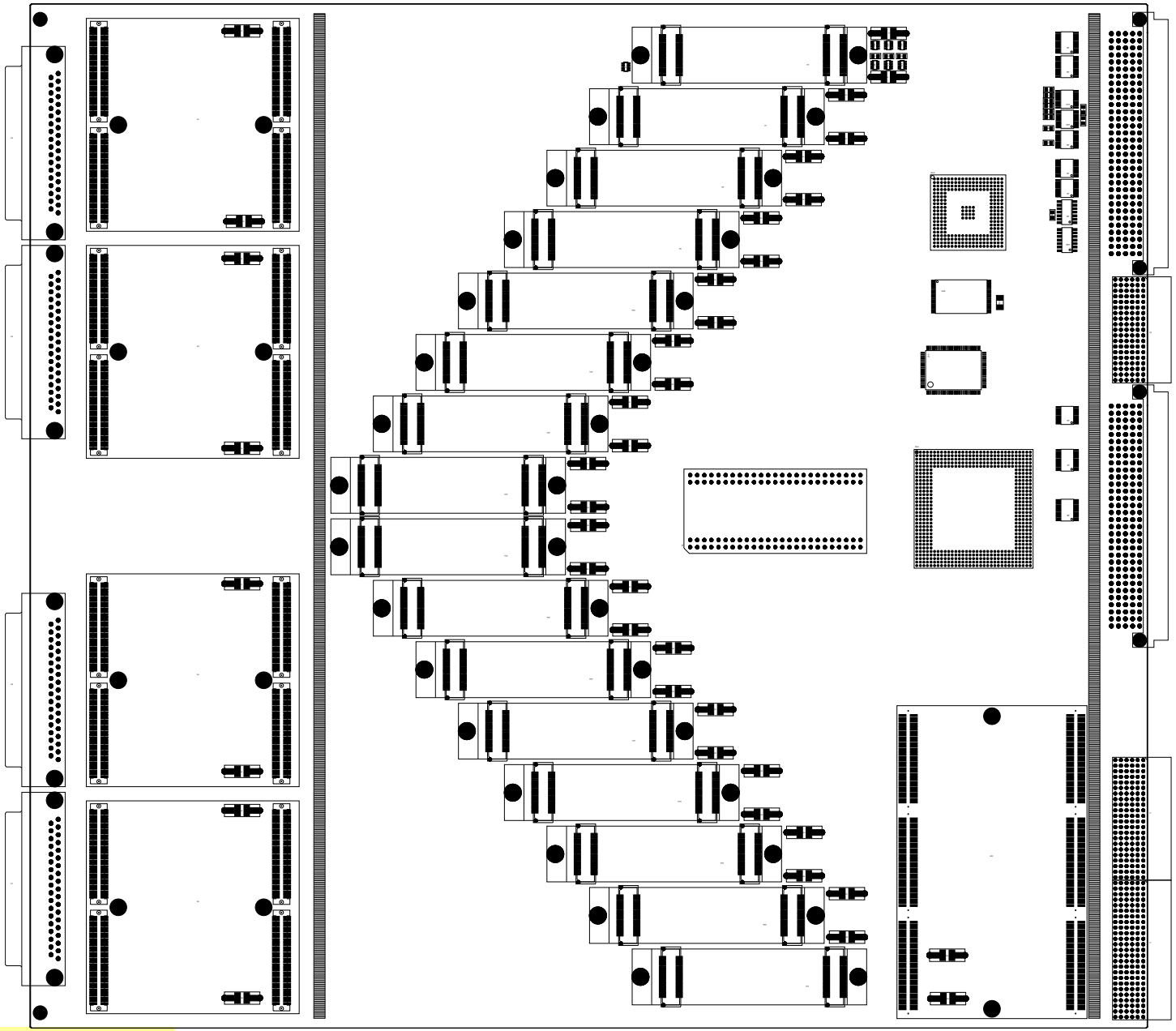
Work to be done:

- Place "small" components: only decouple-Caps, Res-arrays on "solder-side", Mech. "stiff bar"
- Route "analog" signals; "speedy" signals:
(e.g LVDS strip-lines, impedance is not too important, can be matched by termination)

- Distribution of TTC ("differential" across PCB ??)
- Route ReadOut: ReM_FPGA and PipeLineBus

- *PCB...*


Pre-Processor Module
40 cm
36,6 cm
C1
16 an.IN
C2
16 an.IN
Ctrl LEDs
C3
16 an.IN
C4
16 an.IN
16 LRec, 16 Discr (extBCID), +32 DACs (Offs, Thr)
16 LRec, 16 Discr (extBCID), +32 DACs (Offs, Thr)
16 LRec, 16 Discr (extBCID), +32 DACs (Offs, Thr)
16 LRec, 16 Discr (extBCID), +32 DACs (Offs, Thr)
MCM1: 4 chs
MCM2: 4 chs
MCM3: 4 chs
MCM4: 4 chs
MCM5: 4 chs
MCM6: 4 chs
MCM7: 4 chs
MCM8: 4 chs
MCM9: 4 chs
MCM10: 4 chs
MCM11: 4 chs
MCM12: 4 chs
MCM13: 4 chs
MCM14: 4 chs
MCM15: 4 chs
MCM16: 4 chs
CP_a
CP_b
JP
CanBus
TTC Dec
S_RAM
ReM_ FPGA
8 * LFAN
To CP:
32 Drivs (+8 FO)
To JP:
16 Drivs (+3 FO)
VME
Control/ Monitor for 64 chans
Standard VME64x_J1 (5row)
J0 (TTC in)
Standard VME64x_J2 (5row)
Fast ReadOut (PipeLineBus) on "user def"
4fo
4
4
4
4
4
4
4
4
4fo
4*JPfo
4*JP
4*JP
4*JP
4*JP
2*JPfo
Min. Requ. for AMP Connectors: 16*4 mm= 64 mm
10 cm



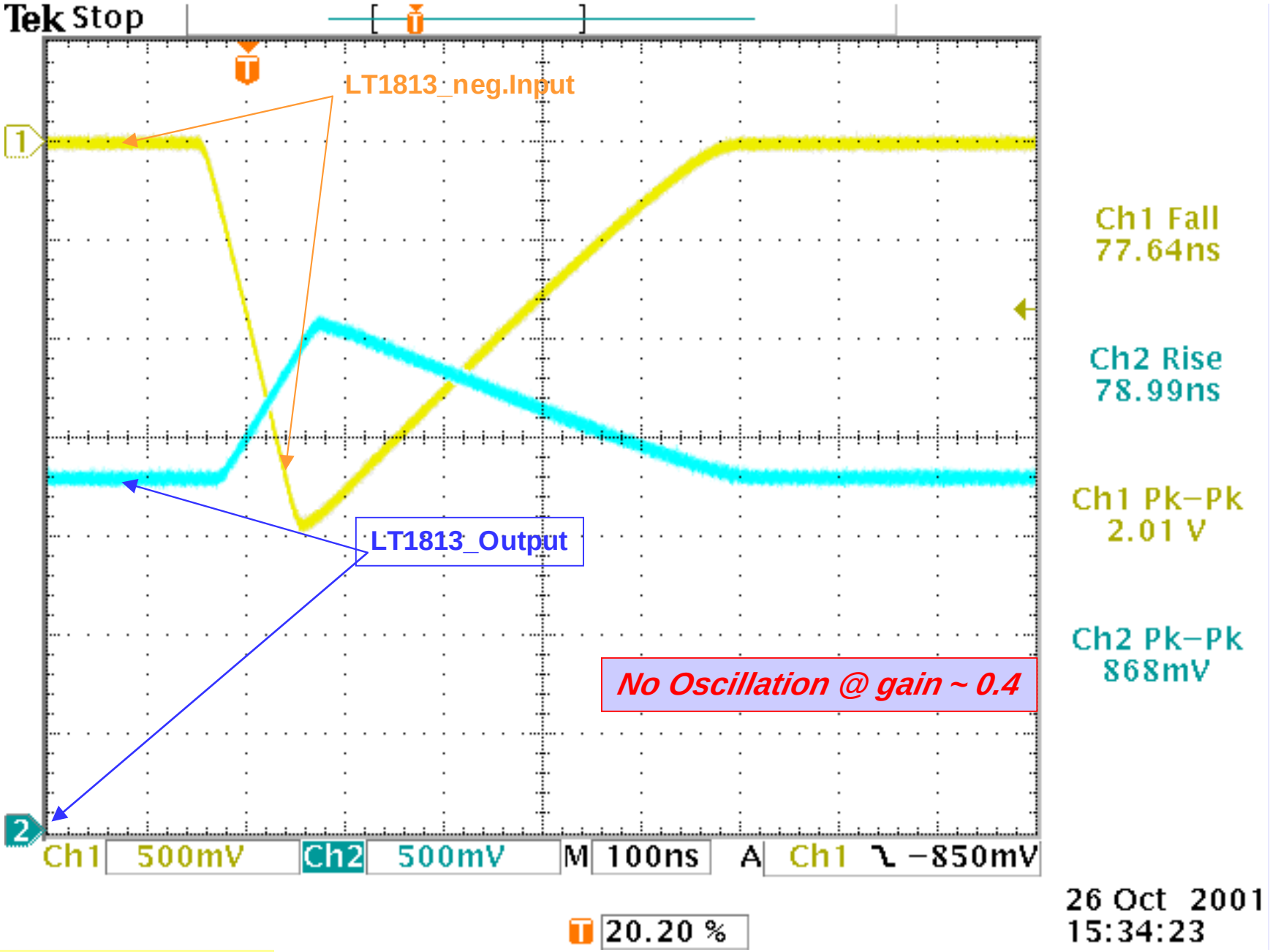
*“AnIn” daughterboard (PCB: 75*75 mm**2)*

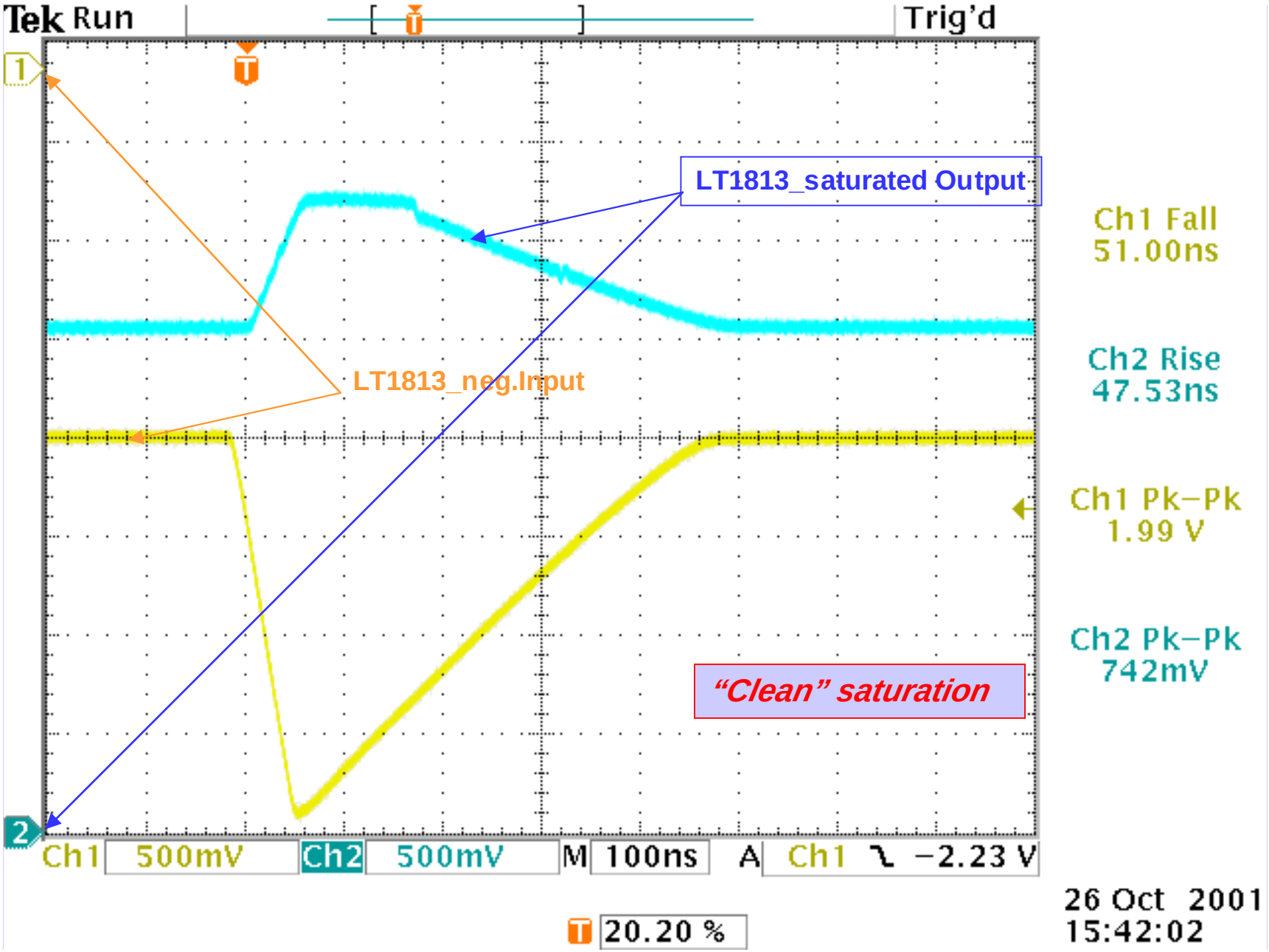
- PCB with “Mezzanine” connectors
- more I/O-pins for better "Xtalk" shielding
- 6 layers
- PowerSupply-Input: +5V dig. separate from +5V analog
- Comparator with "hysteresis"

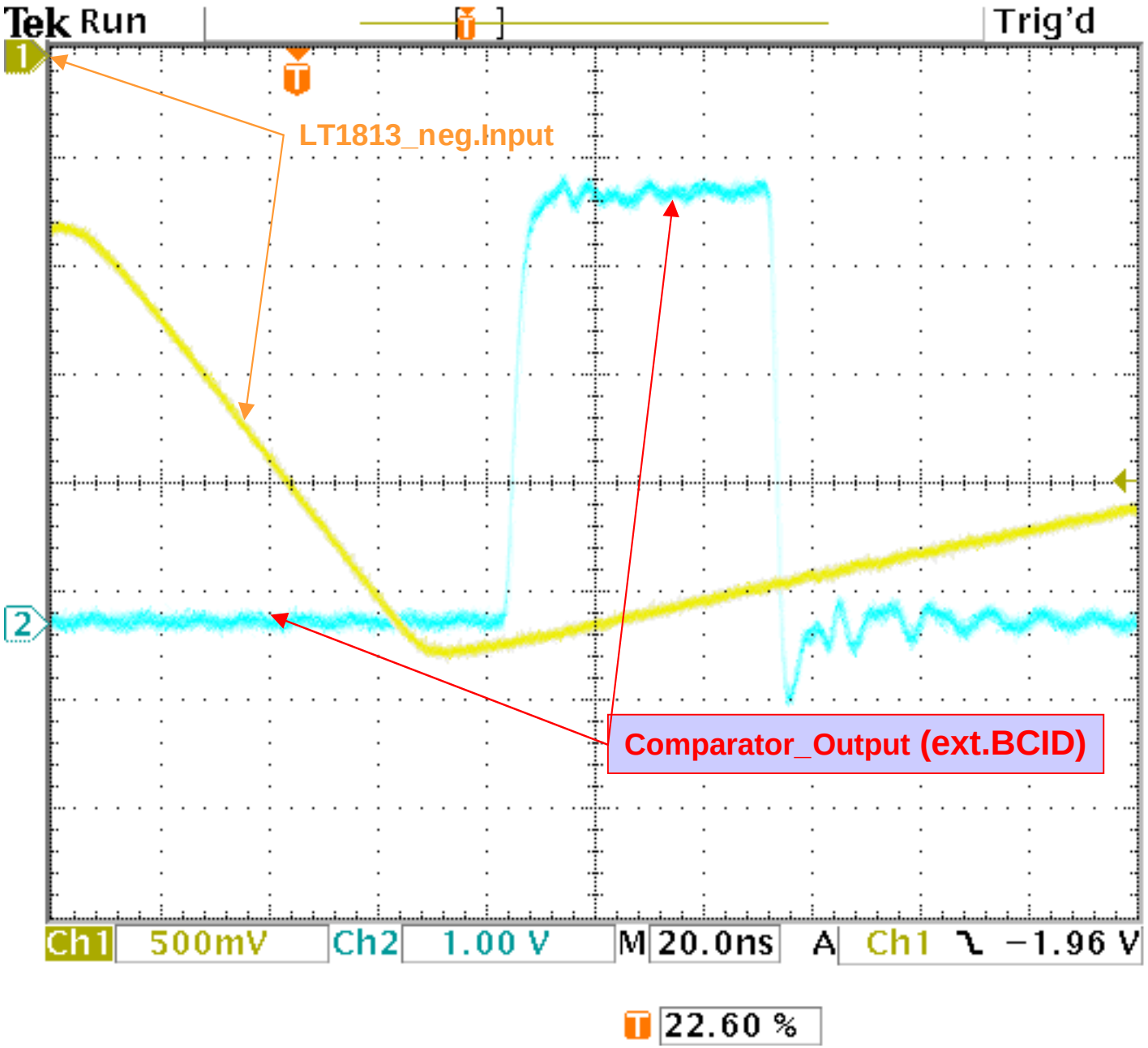
- first results shown @RAL (NoOscill, CleanSat, extBCID), but ...
- Full test- and measurement-program only now: R.Schweike+K.Penno:
- Input from “pulse”-lib.

- FADC-In as ƒ(in-amplitude up into saturation)
- FADC-In as ƒ(offset DAC)
- ext.BCID time-delay as ƒ(thresh. DAC)
- cross-talk (FADC-In: ch.-to-ch., ext.BCID-to-FADC-In)

-> document results.


Tek Stop
LT1813_neg.Input
LT1813_Output
No Oscillation @ gain ~ 0.4
Ch1 Fall
77.64ns
Ch2 Rise
78.99ns
Ch1 Pk-Pk
2.01 V
Ch2 Pk-Pk
868mV
Ch1 500mV
Ch2 500mV
M 100ns
A Ch1 -850mV
20.20 %
26 Oct 2001
15:34:23


Tek Run
Trig'd
LT1813_saturated Output
LT1813_neg.Input
"Clean" saturation
Ch1 Fall
51.00ns
Ch2 Rise
47.53ns
Ch1 Pk-Pk
1.99 V
Ch2 Pk-Pk
742mV
Ch1 500mV
Ch2 500mV
M 100ns
A Ch1 -2.23 V
20.20 %
26 Oct 2001
15:42:02


Tek Run
Trig'd
LT1813_neg.Input
Comparator_Output (ext.BCID)
Ch1 500mV
Ch2 1.00 V
M 20.0ns
A Ch1 −1.96 V
22.60 %
26 Oct 2001
16:17:58

DCS (on PPM board)

- still not clear, what to do :: Candip, PIC18F8680...

- ELMB is not for populated boards.

TTCdec (on PPM board)

- should be ok

LVDS

- LVDS test PCB (CMC board for mod.TestVME)

- PCB manufactured

- test 1021 @ "40 MHz+epsilon" (LHC clock @ 40.8 MHz)

- test XCV50E as "LFan substitute"

- LVDS serializer implementation (meanwhile technically clarified)

- 60 MHz (1023) is "footprint" compatible with 40 Mhz (1021)

i.e. present MCM layout is OK, if to be implemented

- "dies" are available acc. to distributor !

TCM-adapter for PPr

- Schematics of 64x-VME interface done
- TCM-motherboard @HD now, continue el.-mechanics (connectors, mounting)
- TTC distribution for PPr from “bottom” part (use existing PECL drivers)
- use of CAN on TCM ?

- Schedule: finish schematics in Apr.02, layout in May02, PCB in June02

Software for PPr-Hardware

- Purpose: Need "reference" for hardware IN vs OUT on "real-time" path

- Input: "pulse" vectors as in "Video"-memory (from H.Stenzel's lib.)
- Task: emulate PPr functions under "real settings = control input"
- *AnIn pulse forming*
- *FADC-digitisation*
- *ASIC functions (BCID ...) all the way to BC-Mux*

- Output:
- *predict data at "diagnose" points: "PipeMemories"*
- *predict LVDS stream with "tolerance" window for comparison*

- Framework: Follow C++ skeleton / own cooking (rather NOT)?

Material and Sys.-Documentation

• *CoRe - Purchases for the full PPr project (delivered):*

- *front-panel connectors (SubD37)*
- *VME connectors for PPM boards (J1, J2 , J0-cPCI)*
- *cPCI connectors on PPM for LVDS output (B22, B25)*
- *"Mezzanine" connectors for AnIn, LVDS "FanOut"*
- *LVDS-BackPlate: 8_slot units at lower 3U --> see example*
- *ReM_FPGA (XCV1000E)*

[- AMP-cables of 15 m length for "slice test"]

• *Overall Cabling Document (with W.Cleland@HD, Nov.26/27):*

- *preparatory work done (update figures, tables in PPM-spec.)*
- *Excel-file for* **FULL EM-Cal. coverage** *started (lack of time ...)*
- *MUST be done asap !!*

• *Tile-Receivers ? Specification needed for Pittsburgh+DOE.*

Schedule (KIP is moving house May-July02)

• TCMadaptor

- PCB-prototypes (2) loaded => Aug02
- Set-up TTCVi/Vx: asap; who?
- test TTC protocol-chain to destination (i.e. PPM TTCdec) => Sep02

• PPM

- PCB-protoype boards (4) => Jul02
- comp.load (I/O connectors, dPCB connectors, VME,ReM_FPGA) => Aug02 (one PCB)

- "plug-on" components: AnIn, MCM, LVDS-Fanout, TTCdec, (DCS ?)
- "stand-alone" test(only VME; Not yet PLBus) => Sep02
- first "joint" tests ("start of a slice") => Oct02 onwards

• ROD

- Use proto-ROD hardware as configured on mod.TestVME (and PLBus over cable links)
- real ROD as "part of PPM" later)