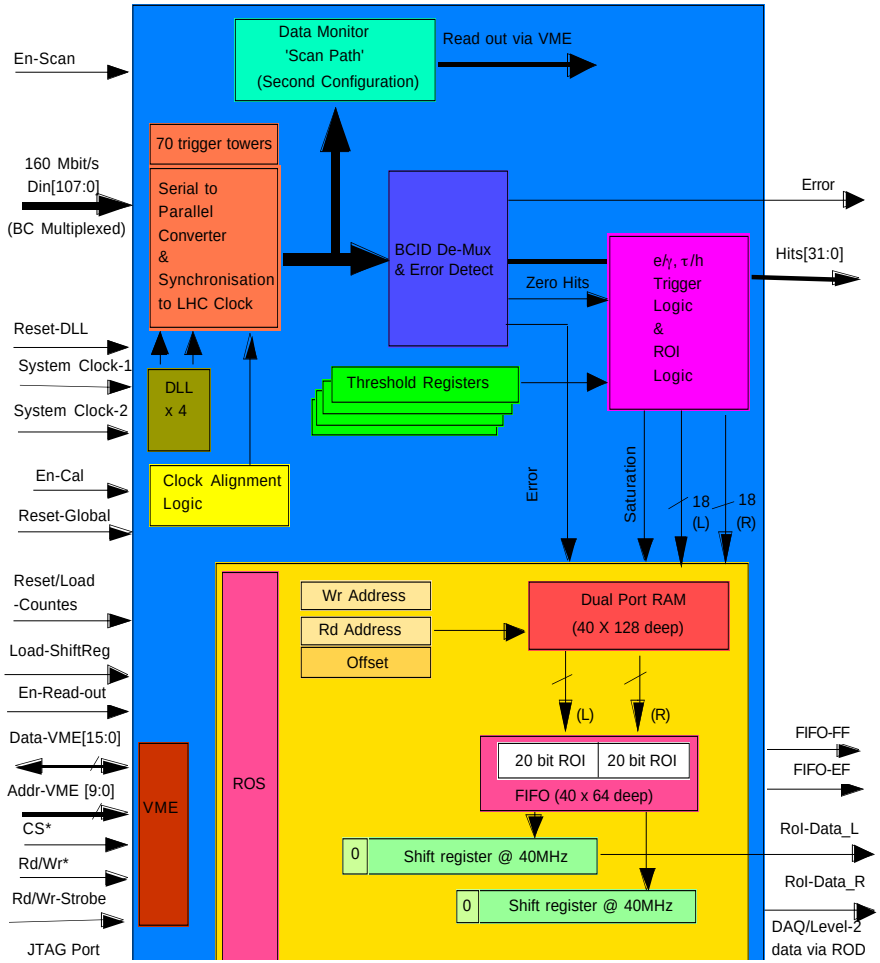
CP “chip” tests using the Generic Test Module (GTM)

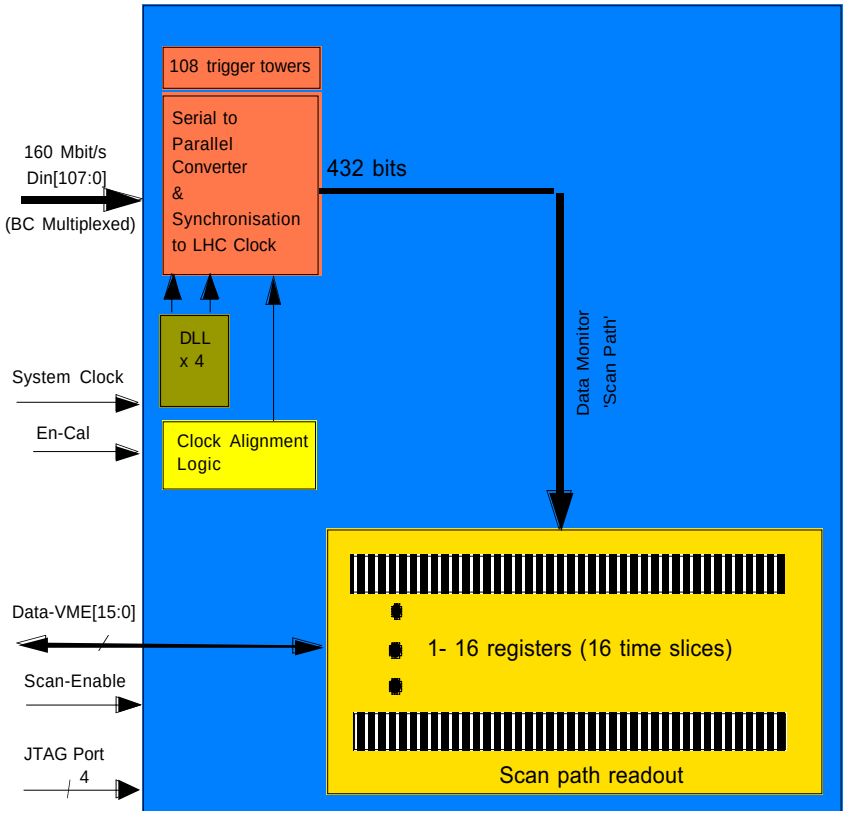
Cluster Processor Chip

- CP Chip will be implemented on XCV1000E-6BG560
- Requirement -1
  - Process 4 x 2 x 2 TT Window
  - Receive BC multiplexed data
    - 108 at 160 Mbit/s
  - Capture and synchronise
  - BC-De mux and error checking
  - e/g, t/h Algorithm
    - Cluster Hits
    - RoIs
  - Readout of RoIs



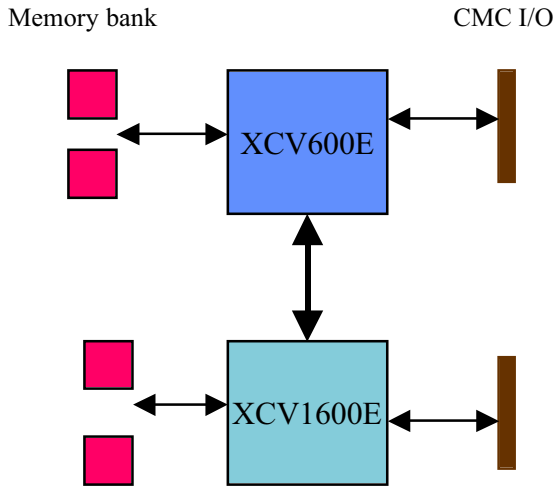
Cluster Processor Chip

- Requirement- 2
  - Set-up and diagnostic Logic (second configuration)



GTM

- Similar architecture to the DSS module



Block Diagram

Test setup on GTM

- FPGA 1 (Two Configurations)
  - Small set of vectors loaded into BlockRAM.
  - Reads test vectors loaded into memory.
- FPGA 2
  - CP chip firmware

Initial Results - Calibration

- All 108 channels calibrate.
  - Receive 160 Mbit/s serial data and automatically select the clock phase to latch the data onto the CP Chip
    - Debugged a number of minor problems.
    - Required the 160 MHz serial to parallel converters to be “hand placed”.

Data Tests

- BlockRAM vectors
  - All 256 vectors passed
- External memory vectors
  - Some errors. Nothing obvious
  - Added “scan path” configuration to aid debugging
    - Configuration to capture the data after de-mux before the data enters the algorithm block

Summary

- GTM useful aid to debugging the CP chip firmware.
- Save time when we get the CPM.