



Towards a slice test DAQ

- the reason why i give this talk today

A few weeks ago i have been asked in one of our internal meetings how a **full** slice test data acquisition will look like.

Especially people wanted to know what data is going to be read, how it is stored, which formats and databases to use how the system is synchronized and and and

My first thought: GOSH

After i spent a week end of thinking about this, i came to to the conclusion that this is a multi layer problem



One perspective to look at the things ahead

It appears to me that there exist four levels at which software is needed.

1. The individual component level, for example the PPrAsic or the MCM testsystem. (-> see W. Hinderers and K.Pennos talk
2. The module level, for example a PPM module
3. The subsystem level, for example the PreProcessor
4. The full slice consisting of several or all subsystems



The component level

Presently PPr hardware is starting to arrive (ASIC,MCM) or is in an well advanced stage of design

The main focus at the moment is to get software ready to test these individual components.

K. Penno is programming firmware for the FPGA's needed and i am working on finally implementing the VME Linux driver for our homebrew CPU into hdmc and to setup hdmc for the component tests.

→ There is a **clear idea** what software needs to be written to test the components arriving. It is also clear to us how to do it



The module level

To test the individual PPM Modules more complex software is necessary.

The key software component will be the RemFPGA which is the device connected to nearly all other components on the PPM module.

The software task at the module level concerning the readout data path is to write firmware which establishes communication with the PPrASIC and does the configure, loading and readout of the registers etc.

D. Kaiser did quite a lot of work on that, but since he will leave the project soon lots of knowledge is lost and it will take time to regain it.



The module level II

Most probably we will be able to use the serial interfaces D. Kaiser and to reuse a smaller subset of his RemFPGA Code to do first PPM module tests

A set of test pulses as analogue input to the system exists
And software to regenerate this pulses using a standard Video card is written → K. Pennos talk.

→ It is **rather clear** what needs to be done to run first tests on the PPM module, although questions remain.



The module level III

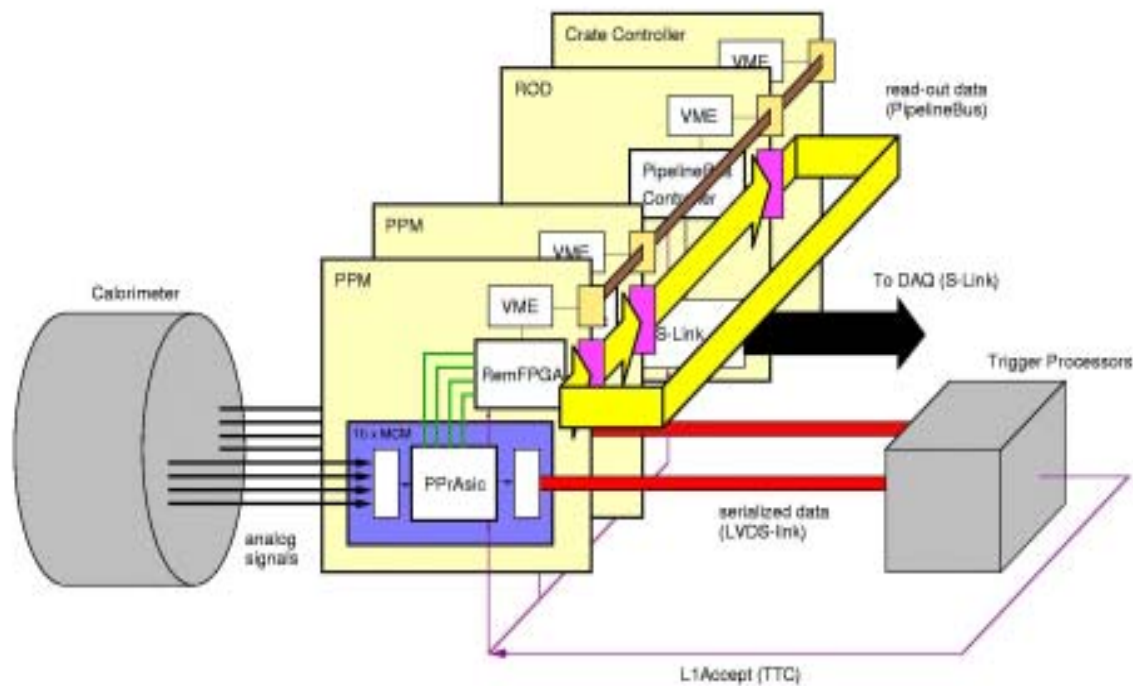
Open Questions

One of them is, as P. Hanke already mentioned, how to compare the realtime data path output with the expectation. We have no simulation so this will be a problem for the later stages of the module testings

Questions remain about how to synchronize the different heads of the video card which we use a analogue input source

The subsystem level

I am now talking about the PPM subsystem, that is





The subsystem level II

To test the subsystem we need to have a full Implementation of the RemFPGA. D. Kaiser did much of This work, nevertheless changes will probably be necessary and it might take time to do them. Additionally it will Take time to debug this code with real hardware.

We need to implement the ROD to collect the data from the pipeline bus. Nothing like this exist so far, except for the Stelzer prototype which probably needs to be redone completely.

So far i think we also havent spent much thought on what to do with the realtime data. How to store, consistency checks

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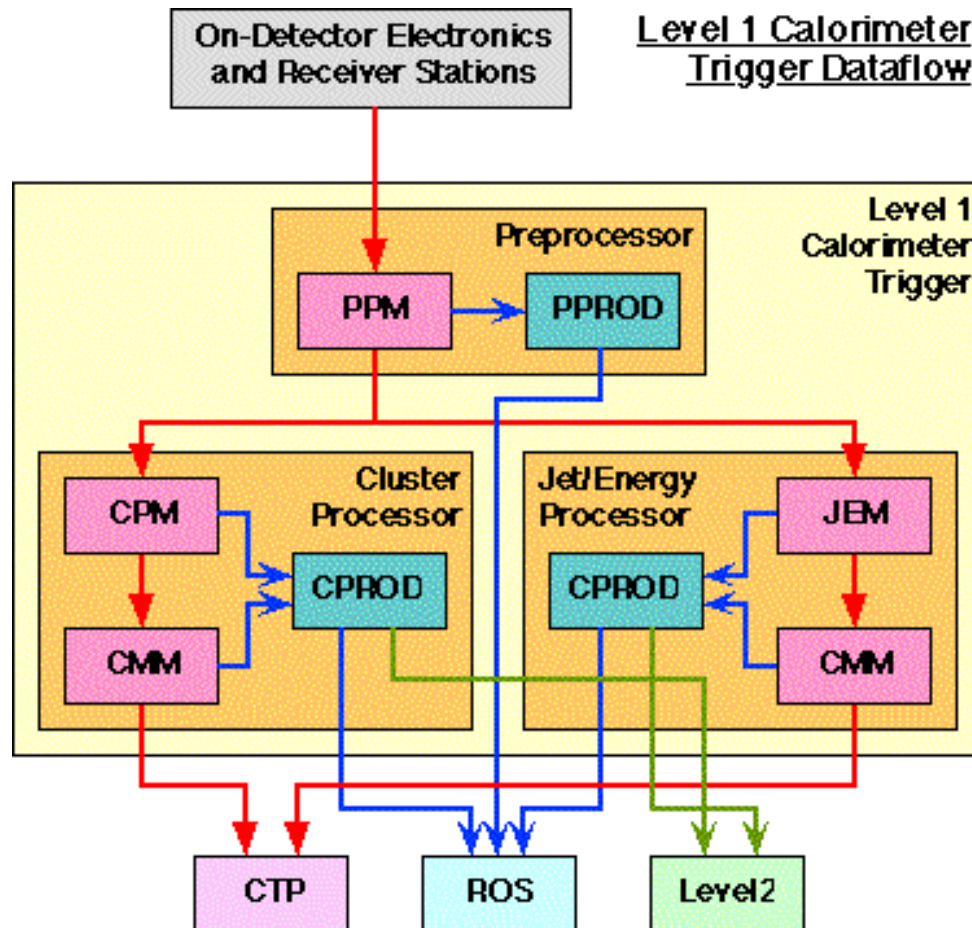
The subsystem Level III

→ It is **somehow clear** what needs

Though there are many open questions on how to realize it.

I am afraid we are still a long way from having a full PPM subsystem (from a software perspective)

The full slice



To summarize:

I am clearly lacking a decent idea on how to get a DAQ and runcontrol software for the slice test

This is not intended as a provocation (i know that much effort is spent by the UK groups in that direction)