
# Slice Tests

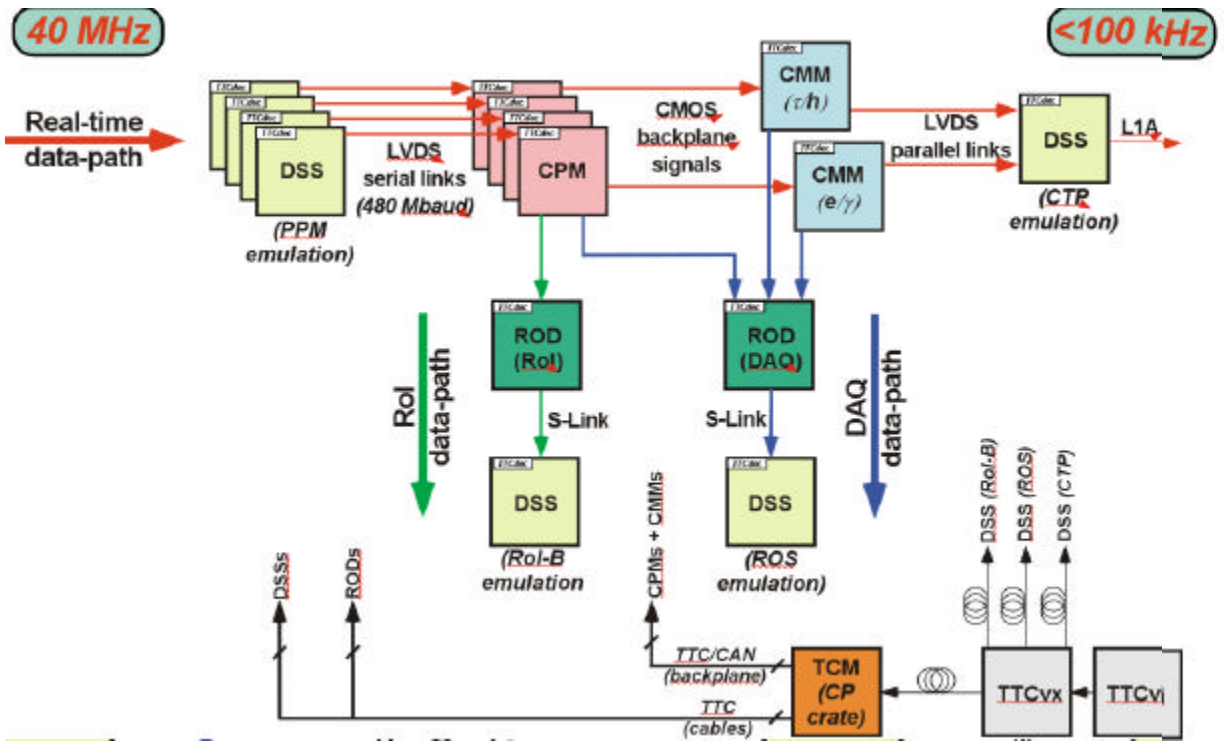
## *Some Planning Issues*

# ASSO – Milestones October 2001

| PBS no | Milestone | Date |
|---|---|---|
| 10.1.2.1 | Start CP/JEP sub-system tests | Jan 2002 |
| 10.1.2.1 | Start "Slice" tests | April 2002 |
| 10.1.2.1 | Completion of "Slice" tests *( f1)* | July 2002 |
| 10.1.2.1.4.8 | FDR for TCM | Oct 2002 |
| 10.1.2.1.4.8 | PRR for TCM | Nov 2002 |
| 10.1.2.1.4.9 | PDR for ROD *(CP/JEP)* | Oct 2002 |
| 10.1.2.1.4.3 | FDR for Processor Backplane *(PB)* | Oct 2002 |
| 10.1.2.1.2.1 | FDR for CPM | Nov 2002 |
| 10.1.2.1.4.3 | PRR for Processor Backplane *(PB)* | Nov 2002 |
| 10.1.2.1.2.1 | PRR for CPM | Dec 2002 |
| 10.1.2.1.3.1 | FDR for JEM | Dec 2002 |
| 10.1.2.1.3.1 | PRR for JEM | Jan 2003 |
| 10.1.2.1.4.1 | FDR for CMM | Jan 2003 |
| 10.1.2.1.4.1 | PRR for CMM | Feb 2003 |
| 10.1.2.1 | Completion of "Slice" tests *( f2)* | April 2003 |
| 10.1.2.1.4.9 | FDR for ROD *(CP/JEP)* | Jun 2003 |
| 10.1.2.1.4.9 | PRR for ROD *(CP/JEP)* | Jul 2003 |
| 10.1.2.1.2 | Full CP sub-system available for System tests | Dec 2003 |
| 10.1.2.1.3 | Full JEP sub-system available for System tests | Jan 2004 |
| 10.1.2.1.2 | Completion of CP sub-system tests | Dec 2004 |
| 10.1.2.1.3 | Completion of JEP sub-system tests | Jan 2005 |
| 10.1.2.1 | Calorimeter trigger available in situ | May 2005 |

# CP Sub-System

## UK Sub-System Tests



# Hardware

- Programme is in two phases - Sub-System Commissioning *(home institutes)* and full Slice Tests *(Heidelberg)*
- Goal is to complete all sub-system tests by ~Q4 2002 – CP and JEP
- Very large number of tested modules/cards are needed before sub-systems can be assembled
- Four stages of readiness for each module/card:
  - (A) still needing design or layout
  - (B) still to be manufactured, assembled and tested *(or purchased)*
  - (C) still to be tested
  - (D) fully-tested and available
- What do we need?

# CP Sub-System & Common Modules – Hardware Requirements

| Module/card | Needed | Design/ Layout | Manufacture/ Purchase | Number awaiting test | Tested | Comments |
|---|---|---|---|---|---|---|
| | | | | | | |
| DSS | 10 | - | 0 | 6 | 4 | } Populates 1 full CPM *(80 channels)* |
| CMC LVDS Tx Card | 20 | - | 16 | 0 | 4 | } and 2 partial CPMs *(40 + 40 channels)* |
| CMC Generic I/O Card *(GIO)* | 3 | Layout | 3 | 0 | 0 | CPM-CMM tests via PB; CTP-D emulation |
| CERN TTC Test Card | 4 | - | 0 | 0 | 4 | Only usable on DSS - optical input |
| TTCdec Interposer | 8 | - | 6 | 0 | 2 | Needed to allow use of TTCdec with RODs |
| TTCdec | 30 | Design | 20 | 7 | 3 | Re-design needed for new TTCrx footprint |
| LVDS 4-channel Link Cable | 126 | - | 0 | 0 | 160 | 15m - from 6 PPMs -> (2+2 CPMs + 2+2 JEMs) - from HD |
| CPM | 4 | - | 4 | 0 | 0 | 2 fully-populated, 1 partially-populated |
| CPM Emulator 1 *(CPME1)* | 4 | Design | 4 | 0 | 0 | Sources/sinks 160 Mbit/s serial data *(firmware?)* |
| CPM Emulator 2 *(CPME2)* | 4 | - | 4 | 0 | 0 | } Sources/sinks HIT data for CMM via PB |
| CMM Emulator *(CMME)* | 2 | Layout | 2 | 0 | 0 | } and provides CPM-CMM PB testing |
| CMM | 4 | - | 4 | 0 | 0 | 2 for CP sub-system, 2 for JEP sub-system |
| Rear Transition Module | 4 | Layout | 4 | 0 | 0 | Sources/sinks CMM I/O data *(crate dimensions awaited)* |
| TCM/ALC | 7 | - | 4 | 0 | 3 | 2 for UK, 2 for Heidelberg, 2 for Mainz, 1 spare |
| ROD *(6U)* | 8 | - | 6 | 0 | 2 | } Slice Tests - 3 for CP + 4 for JEP |
| CMC G-Link Rx Card | 8 | - | 4 | 0 | 4 | } sub-systems + 1 spare *(CMM firmware needed)* |
| S-Link Tx/Rx Card-set | 7 | - | 1 | 0 | 6 | Slice Tests RODs - 3 for CP, 4 for JEP |
| S-Link Rx PCI I/F | 7 | - | 1 | 0 | 6 | Slice Tests ROSs - 3 for CP, 4 for JEP |
| VME Mount Module *(VMM)* | 5 | - | 4 | 1 | 0 | Adapts 6U CPU to 9U VME-- crate - CP 2, JEP 2 + 1 spare |
| CPU *(Concurrent)* | 6 | - | 2 | 0 | 4 | Slice Tests - 2 VME crates + 4 VME-- crates |
| TTCvi + TTCvx | 2 | - | 0 | 0 | 2 | Slice Tests + UK Test System |
| 6U VME crate | 3 | - | 1 | 0 | 2 | Slice Tests + UK Test System |
| 9U crate/PB | 2 | - | 0 | 2 | 0 | } 1 for Slice Tests |
| 9U crate PSU | 2 | - | 0 | 0 | 2 | } + 1 for UK Test System |
| Optical fibres *(TTC + S-Link)* | ~15 | - | ~10 | 0 | ~5 | Lengths? |

# Some Observations

- There is a large amount of hardware to test and assemble into 2 sub-systems ® a similarly large amount of firmware and software also needed
- The common modules *(ROD, CMM, TCM)* will be tested in the UK, so their integration with the JEP system may be most efficiently achieved there
- Golden Rule - only when both sub-systems are "under control" move to Heidelberg
- Because of the magnitude of the programme, it is proposed to take a critical look at the scope and duration of the two phases
  - Have the objectives of the tests really been fully defined – in particular, for sub-systems?
  - It may be wise to set more realistic goals for each phase to match available resources
  - "Deferral" is flavour of the month – overall programme may need to be lengthened

| ID | Task Name |
|---|---|
| 1 | ***CP SUB-SYSTEM PROGRAMME*** |
| 2 | |
| 3 | **CPM Prototype** |
| 4 | JTAG tests (RAL) |
| 5 | VME tests, etc |
| 6 | Standalone tests - 1 |
| 7 | Standalone tests - 2 |
| 8 | Commission CMMs 2-4 |
| 9 | ***CPMs available for CP sub-system tests*** |
| 10 | |
| 11 | **Common Merger Module (CMM)** |
| 12 | JTAG tests |
| 13 | VME tests, etc |
| 14 | ROD tests, etc |
| 15 | Real-time (emulation) tests -1 |
| 16 | Commission CMMs 2-4 |
| 17 | Real-time tests -2 |
| 18 | ***CMMs available for sub-system tests*** |
| 19 | |
| 20 | **CP (and JEP?) sub-system tests** |
| 21 | |
| 22 | **Phase 1 "Slice" Tests (Heidelberg)** |
| 23 | |
| 24 | ***Phase 1 "Slice" tests complete (Milestone)*** |
| 25 | |