CPM Prototype Hardware & Test Cards

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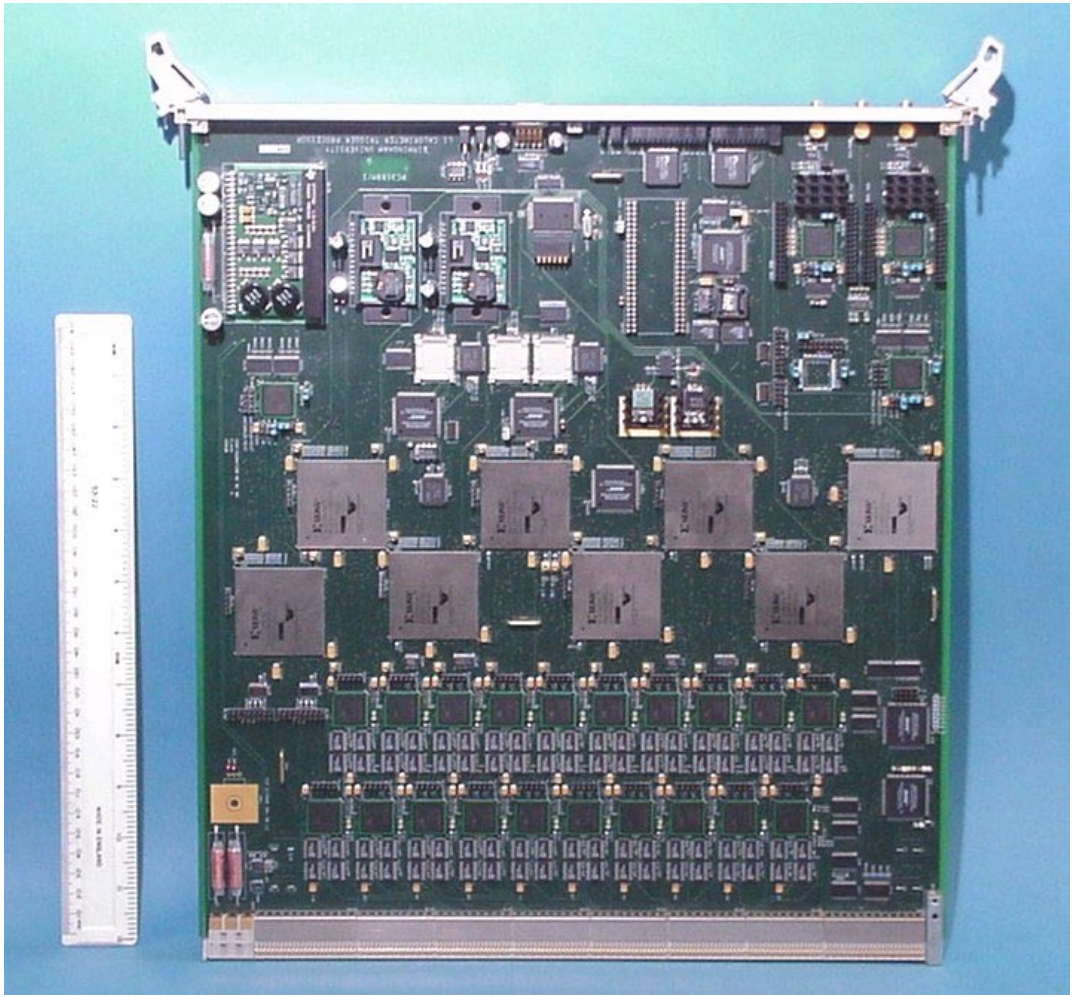

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Statistics

4 bare PCBs made

1 PCB assembled, undergoing tests.

10 signal layers + 6 power planes

0.1mm wide tracks, 0.2mm pitch.

8000 nets

14000 vias , 23,000 pins.

2000 R & Cs

8 XCV1000E and 24 XCV100E VirtexE FPGAs
+ 6 ALTERA PLDs + 80 LVDS DeSers

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Documentation

Hardware User Guide
http://www.ep.ph.bham.ac.uk/user/staley/CPM_USER.pdf

PCB Modifications
/user/staley/CPM_MODS.pdf

Configuration Controller CPLD
/user/staley/ CPM_FLASH_controller/

Programming Memory Map
/user/staley/CPM_MM.pdf

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Recent Progress

Clock Distribution using PLLs performing as intended.

CAN uC overheating / Geographical Addressing prob. fixed →

VME interface working

- Access to ID , Revision, Control and Status registers
- R/W and Erase FLASH memory.
- All Serialiser FPGAs configure . →
- Serialisers connected to VME

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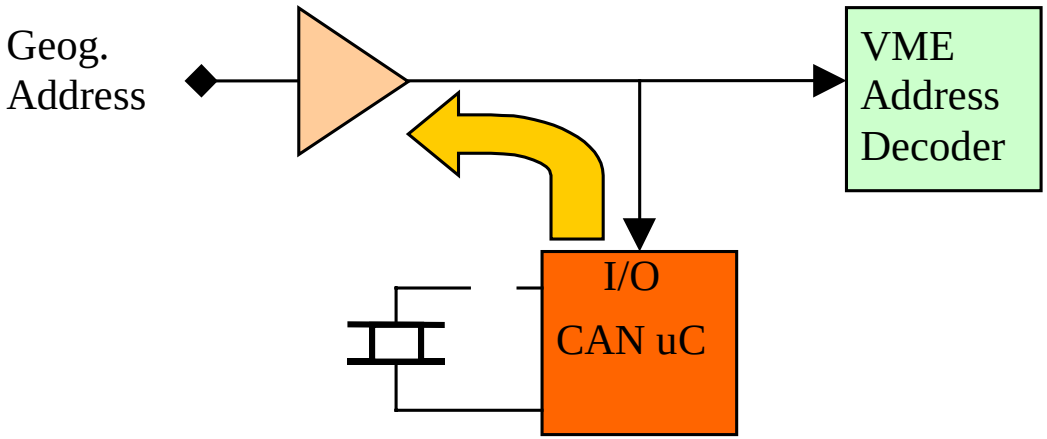
CAN uC

CAN uC clock oscillator pin was unsoldered , giving an intermittent contact with crystal resonator.
Incorrect operation caused CAN uC to over-heat and also to dump current onto the Geographical Address lines:



More robust design … add resistors in series with CAN uC 'inputs'.

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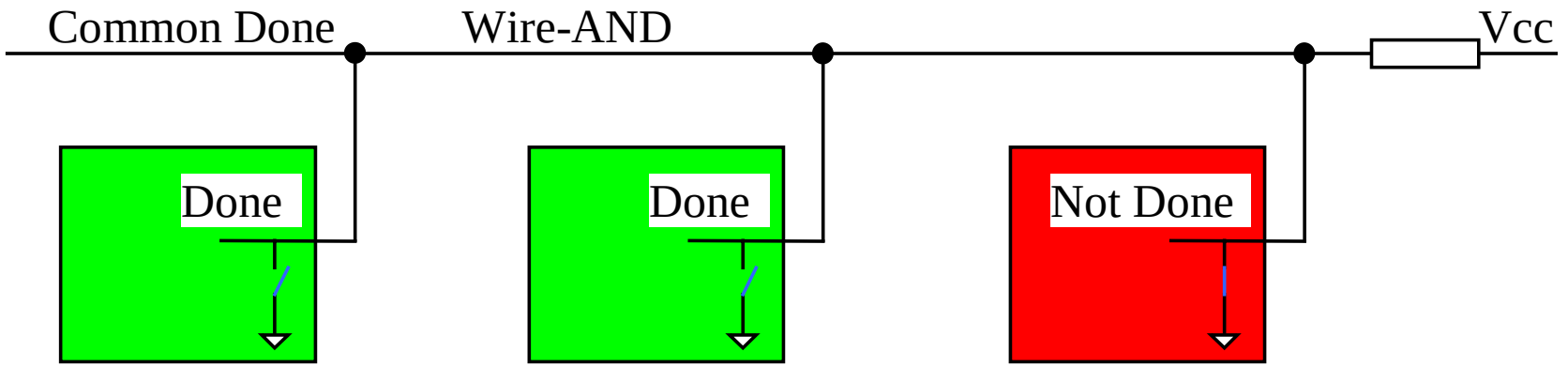
FPGA Configuration Experience

As suggested in various XILINX notes, groups of FPGAs may have their configuration DONE pins tied together:



However, XILINX FPGAs signal 'configuration completion' by releasing the DONE pin … and then wait for this pin to be released externally! Not very good for fault tolerance , development work …

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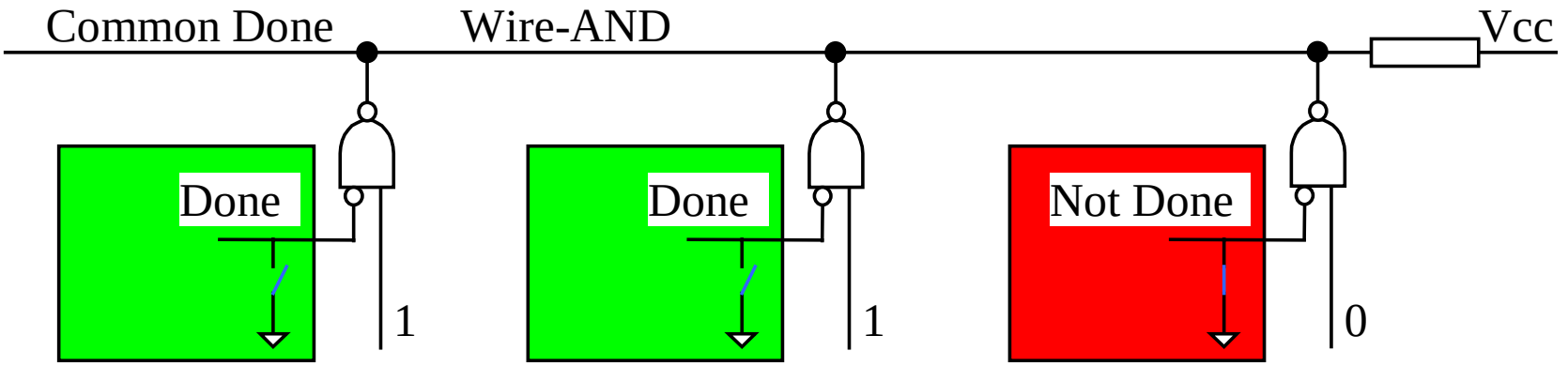
Luckily , this default behaviour can be over-ridden in the configuration file, to make the FPGAs 'wake-up' before DONE is released. (Keywords - BitGen , GTS , GSR and GWE).

For the current design, the FPGA Configuration Controller will now finish after sending a fixed length of data

Next revision of CPM design will condition the DONE signals:



Mechanical Items

Mechanical Stability. PCB is too flexible.

Unresolved. No means to fit strengthening bars.

Status of Birmingham Crate

Longer Guide rails.

Ground Power pins (except CPU slot 1)

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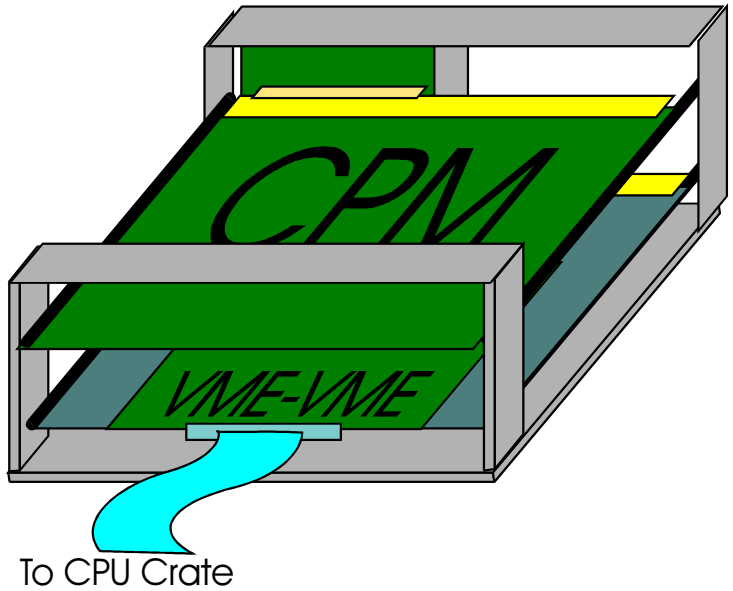
Test Access

Crate Extender , Pizza Box or …

Pizza-Box
+ Standard parts, small custom 'backplane' connecting VMM to CPM.



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Power Supplies

CPU + TTCvi in separate 6U crate to the 9U test crate, connected by VME-VME link (Bit3 - SBS)

- Avoids re-booting CPU when hardware has to be removed

However , powering-up the two PSUs (ETA) in the 9U crate sometimes (1 in 3) shuts-down the 6U CPU crate supply (Wiener).

- Add inline filters. (10^{th} power-up , Wiener shut down)
- Stagger power-up of 9U crate supplies.
- Replace 6U CPU crate.

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Next

- Serialiser in Playback mode to Generate 160Mb/s data. (Requires TTCRx Controller to be working)
- Configure CP FPGAs & test.
- Configure ROC and Hit FPGAs & check Readout
- Fit TTCdec card and test TTCRx I2C Interface
- Validate transmission of all 160Mb/s signals.
- …

→ Subsystem tests.

Test Cards

CMM slot adapters
- Checking Processor Hit outputs with DSS/GIO.

1 prototype , 5 more to be ordered

CPM slot adapters
- Checking CMM Hit inputs with DSS/GIO.

1 prototype made.

CPM loop-back adapters
- Testing 160Mb/s links at Backplane connector.
  Configurable links + Logic Analyser.

5 to be ordered

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Summary

Making steady progress with development.

- VME-- Interface working
- Reliable access to FLASH memory
- FPGA configures from FLASH memory

Very difficult to probe module inside crate

9U Crate Power supplies need taming.

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