CPM Test Progress

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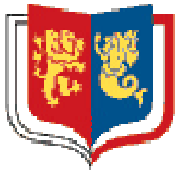
Plans



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Setup in the Lab

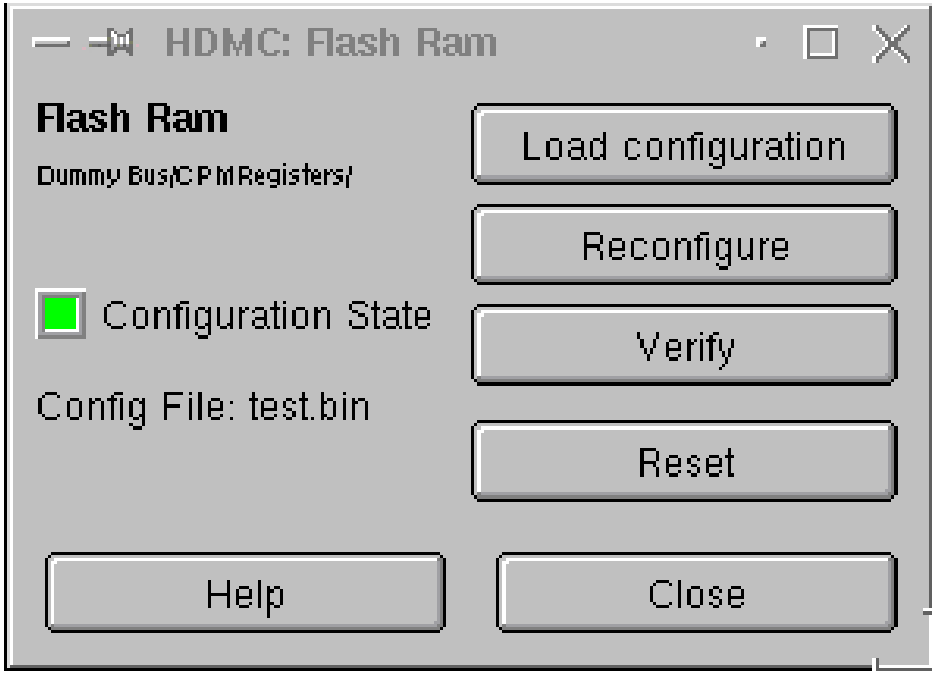
- One 9U L1 crate with VMM with Bit3 + CPM + TCM
- One 6U crate with Concurrent CPU + TTCvi + TTCvx + Bit3
- One PC with Linux 7.2 + HDMC

Test done so far

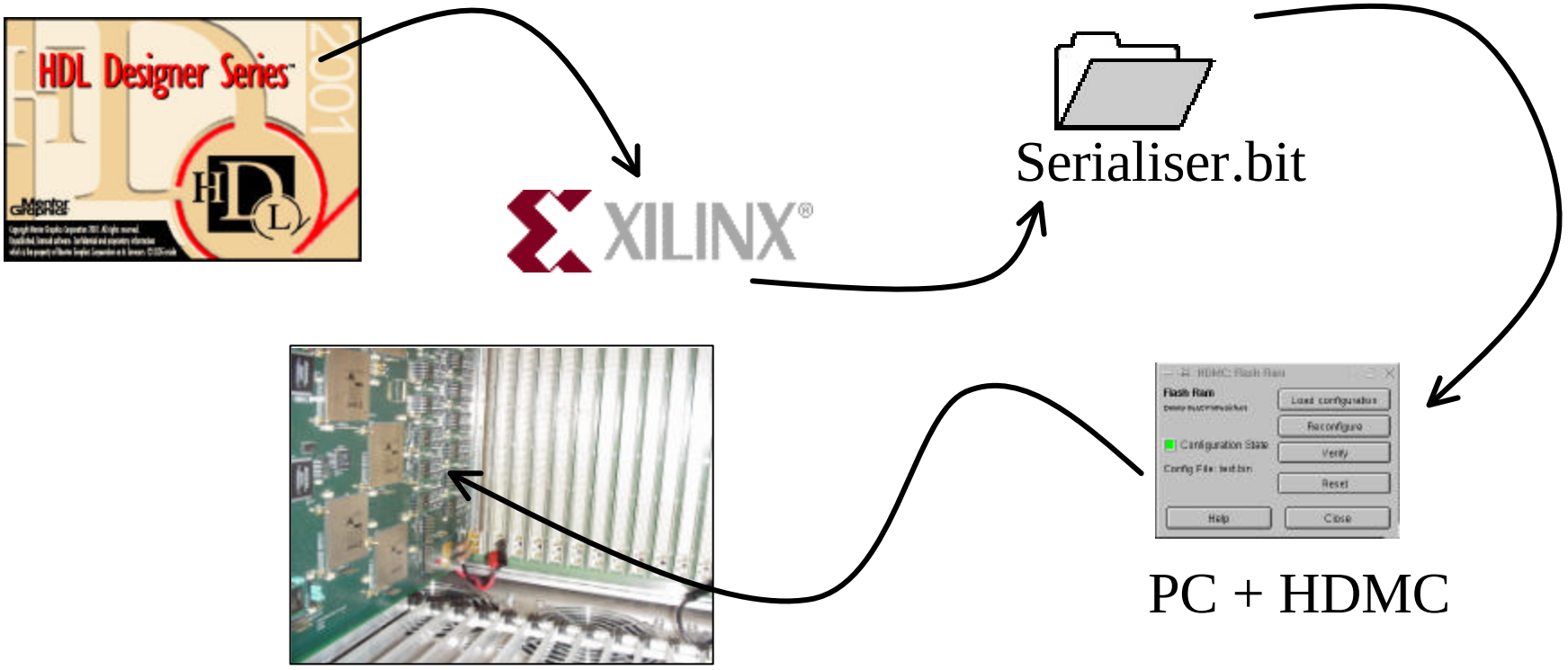
- TCM:
  - Id read [yes]
  - F/W version read [yes]
- CPM:
  - Recover Motherboad ID, [yes]
  - F/W version (GeoAddr by-passed) [yes]
  - Write to Control Register [yes]
  - Write to FlashRam F/W [yes]
  - Serialisers all loaded [yes]
  - Serialisers ID recovered [yes]
  - PlayBack Memory loaded [no]

New part for HDMC: CpFpgaFlashRAM

- Ask for Configuration binary File
- Verify: Read back file from Flash Ram
- Reset: erase Flash Ram
- Bytes are swapped before downloading to take care
  of the swapped format of the PROM port
- Only CPM dedicated



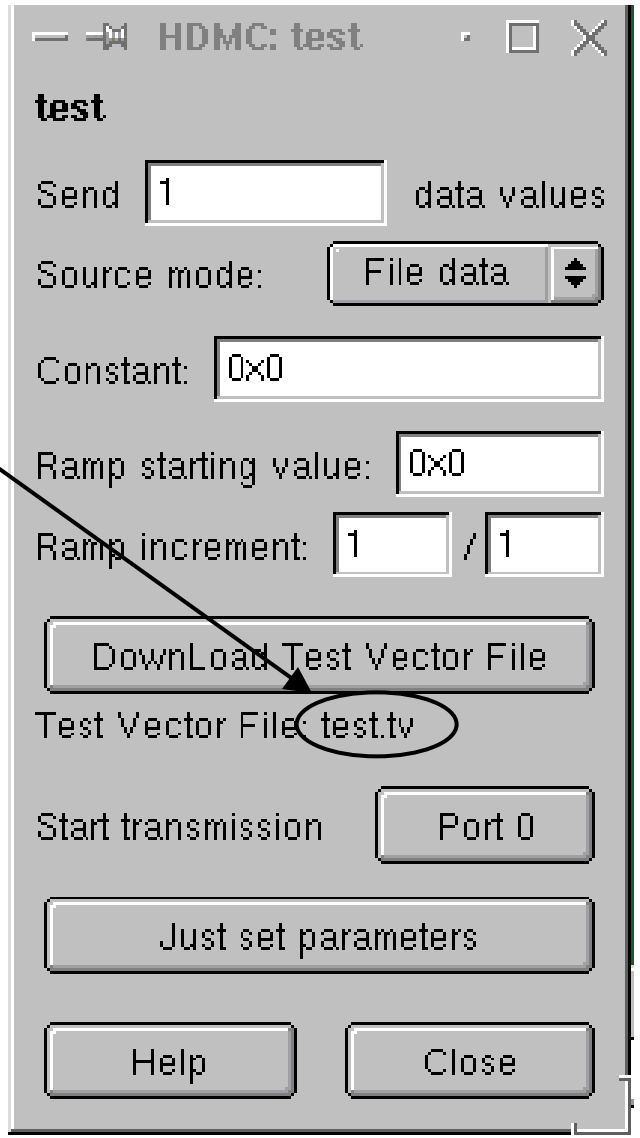
Fpga handling



- Several dummy firmwares have been written first to test the controller between the Flash Ram and the Fpga.
- Firmware binary file formatted in order to start tests on only one serialiser

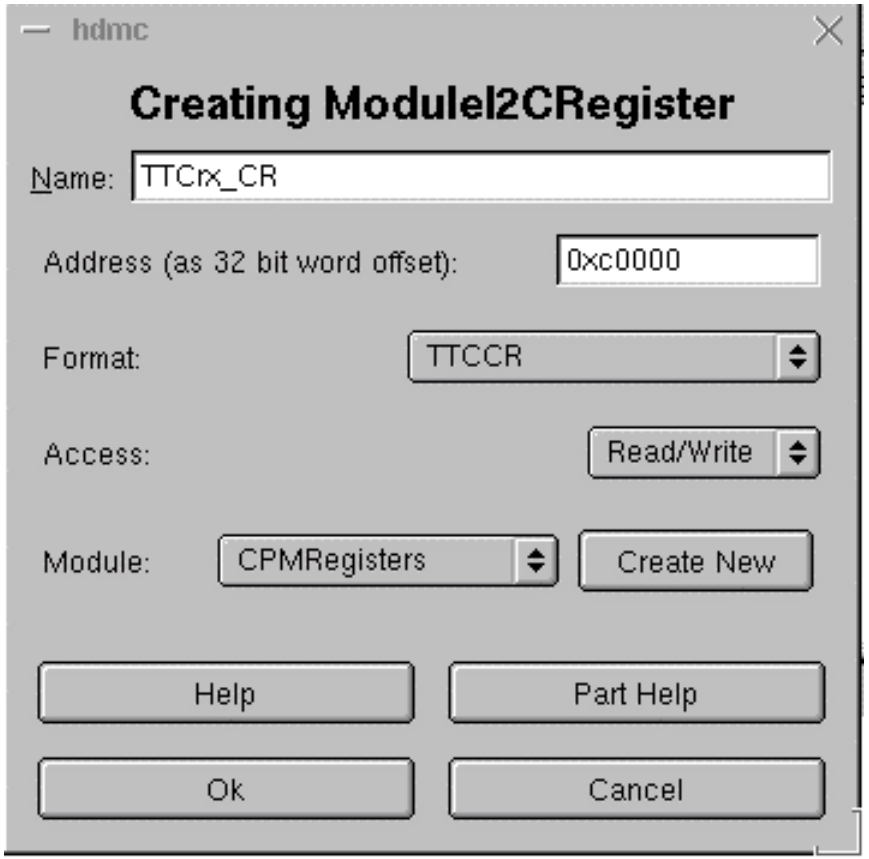
New Part: DataSourceTV

- Load an external file of hex Test Vectors values, to be used inside a RAM for ex.
- CPM application: testing Real Time Path between Srl and CP chips



Part file, to be done: ModuleI2CRegister

- Read/Write to TTCrx register via I_2C access
- Use of only 2 registers to do the access is hidden in the part and I_2C controller
- Set of TTCRx registers: Timing and Control registers



Next steps

- One then 7 Cp chips to be downloaded
- Load Memories and play back data
- Check Real Time Data Path + connectivity
- Load and debug others F/Ws: Hit, ROC
- Modules Services of CPM
- TTCrx testing (I2C)
- Add DSS and test LVDS inputs