ATLAS Level-1 Calorimeter Trigger

Joint Meeting @ Stockholm, Jul.2002

Pre-Processor (System Issues)

- *Status of the PreProcessorModule*
  - *sub-components*
- *other PreProcessor items*
  - *System parts @ Atlas*
  - *Test Parts*
- *Material, Misc...*
- *Planning*

Status of the PPModule

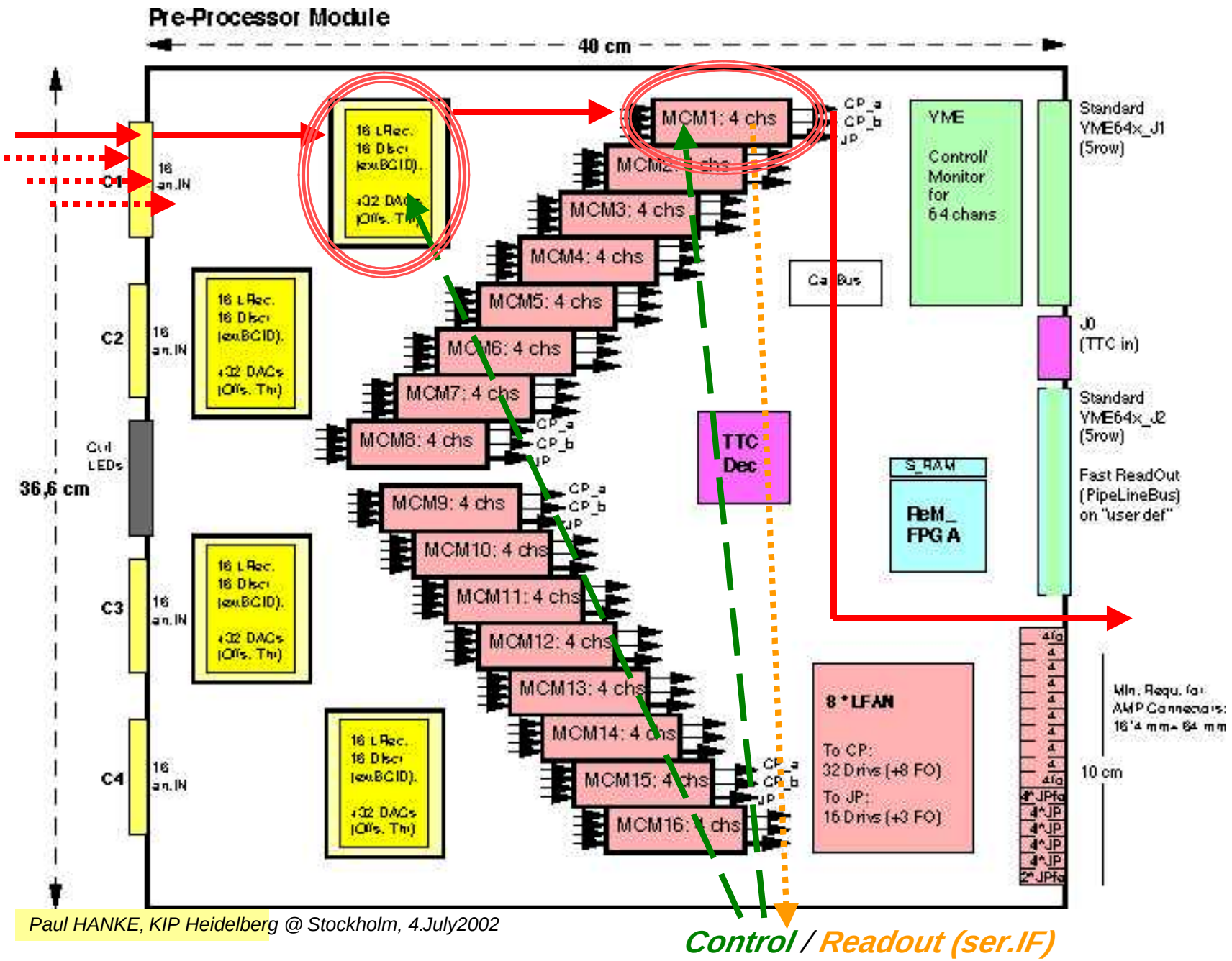
- **Schematics:** *Engineers/Technicians to date busy on test hardware, but*

  - Commercial parts in libs (SubD37, cPCIs, VMEs)
  - AnIn, MCM, TTCrx_dPCB defined in libs
  - VME connected
  - work on connectivity from front-panel through ... to cPCI
  --- >>> little more since March02 @ HD

  - ReM_FPGA on 1.27mm pitch BGA(560 pins)
  - LVDS daughterboard to be defined (see later)

- **PPr "CORE" test:** *AnIn, MCM (+ASIC+LVDS), Ser.Readout*

  - priority before PPModule (due to human resources !)
  - status given by R.Achenbach and K.Penno



Control / Readout (ser.IF)

- **AnIn daughterboard**
  - *under test*

- **MCM**
  - *under test*

- **PPModule board**
  - *start PCB as soon as resources are free,*
  i.e. now, since “test PCBs” are done.

- **LVDS serializer implementation** *(choice: see later)*
  - *60 MHz (1023) die is "footprint" compatible with 40 Mhz (1021)*
  i.e. present MCM layout is OK !
  - *"dies" are available acc. to distributor !*

- **LVDS daughterboard (cable driver)**
  - *must be started soon; last sub-component for PPModule*
  - *need to prove usability of XCV50e in ongoing tests*

- **ReM_FPGA and PipeLineBus access**

- ReM_FPGA code development (D.Kaiser) started “from scratch” !
-> Verilog for ReM_ASIC not usable ?!

- code has not been implemented on hardware and checked

*- code size for XCV1000e changed in last devlopment stages (*2 too big ?)*

- DK promised to carry on part-time: work over code for optimization,
e.g many resources allocated in parallel
*where not necessary (* 32 SerIFs)*

- no feedback yet since May02 ...

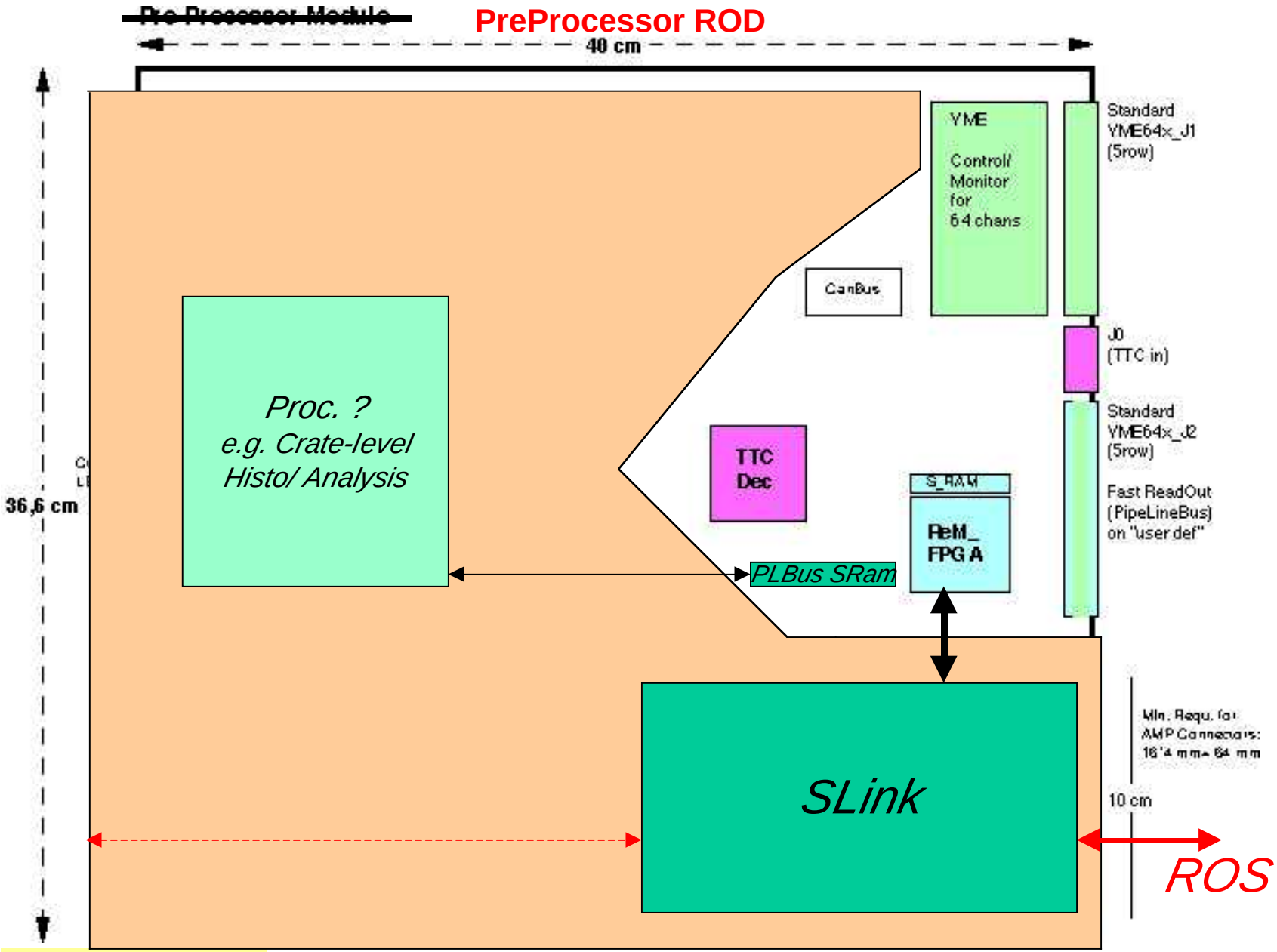
Other Pre-Processor Items

System parts @ Atlas

- **The TCM-adapter for PPr**
  - *motherboard available from RAL*
  - *no resources yet to take PPr-adaptor further*

- **LVDS crate-backplate** *("old")*
  - *commercial solution from ELMA-Trenew:*
  8 PPM--slots (3U) for LVDS throughput (B22, B25) with cable-shrouds for AMP-cables

- **The PPr_ROD** *as "part of PPM":*
  - *final 9u ROD not yet started*
  - *code for XCV1000E as "PLBus Master" (cont. B.Stelzer's work, who ?)*
  - *layout -> see figure*


Pre Processor Module
PreProcessor ROD
40 cm
36,6 cm
VME
Control/
Monitor
for
64 chans
CanBus
Standard
VME64x_J1
(5row)
J0
(TTC in)
Standard
VME64x_J2
(5row)
Fast ReadOut
(PipeLineBus)
on "user def"
Proc. ?
e.g. Crate-level
Histo/ Analysis
TTC
Dec
S_RAM
ReM_
FPG A
PLBus SRam
SLink
10 cm
ROS

Test Parts

- **Linux "homebrew"** *for in-house tests (O.Nix+K.Penno+K.Schmitt)*

- **LVDS test PCB** *(CMC board for mod.TestVME system):*
  - *manufactured and Comp.-loaded*
  - *test 1021 @"40 MHz+epsilon" (LHC clock @ 40.08 MHz)*
  - *decide on version for MCM (1021@40 MHz, 1023@40-60 MHz)*

  ==>> propose 1023 (40-66 MHz) for ATLAS

  - do "Slice-test" MCMs with 1021 (we have 'em)

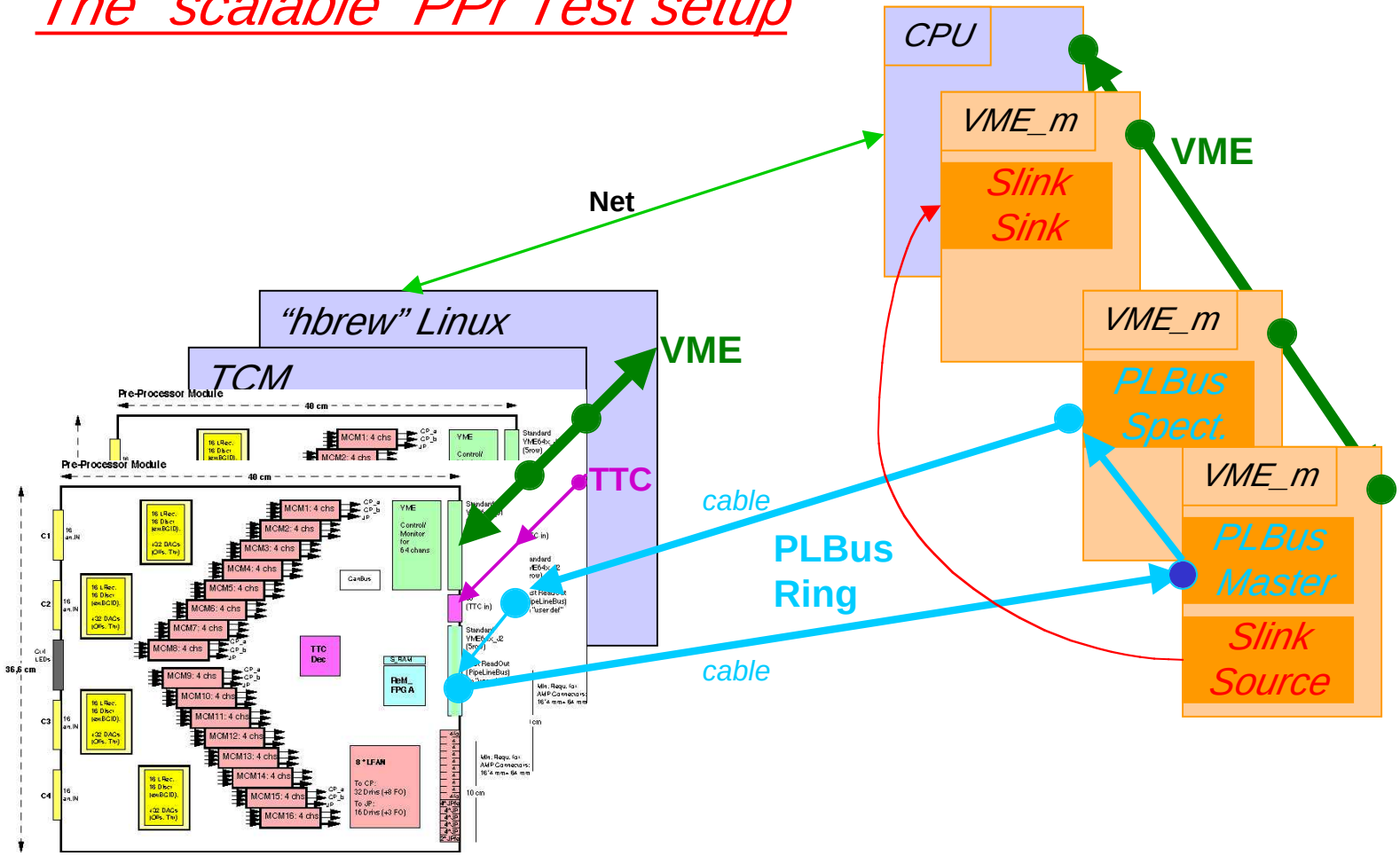
  -->> bond 1or 2 MCM with "1023 die-samples" and test to prove exchangability
  - *test XCV50E as "LFan substitute"*

- **pre-ROD (as before on mod.TestVME)**
  - *use CMC with XCV300 loaded with B.Stelzer's "ROD-code"*

  -->> "PLBus Master"
  - *configure PLBus ring with "short" cable segments*

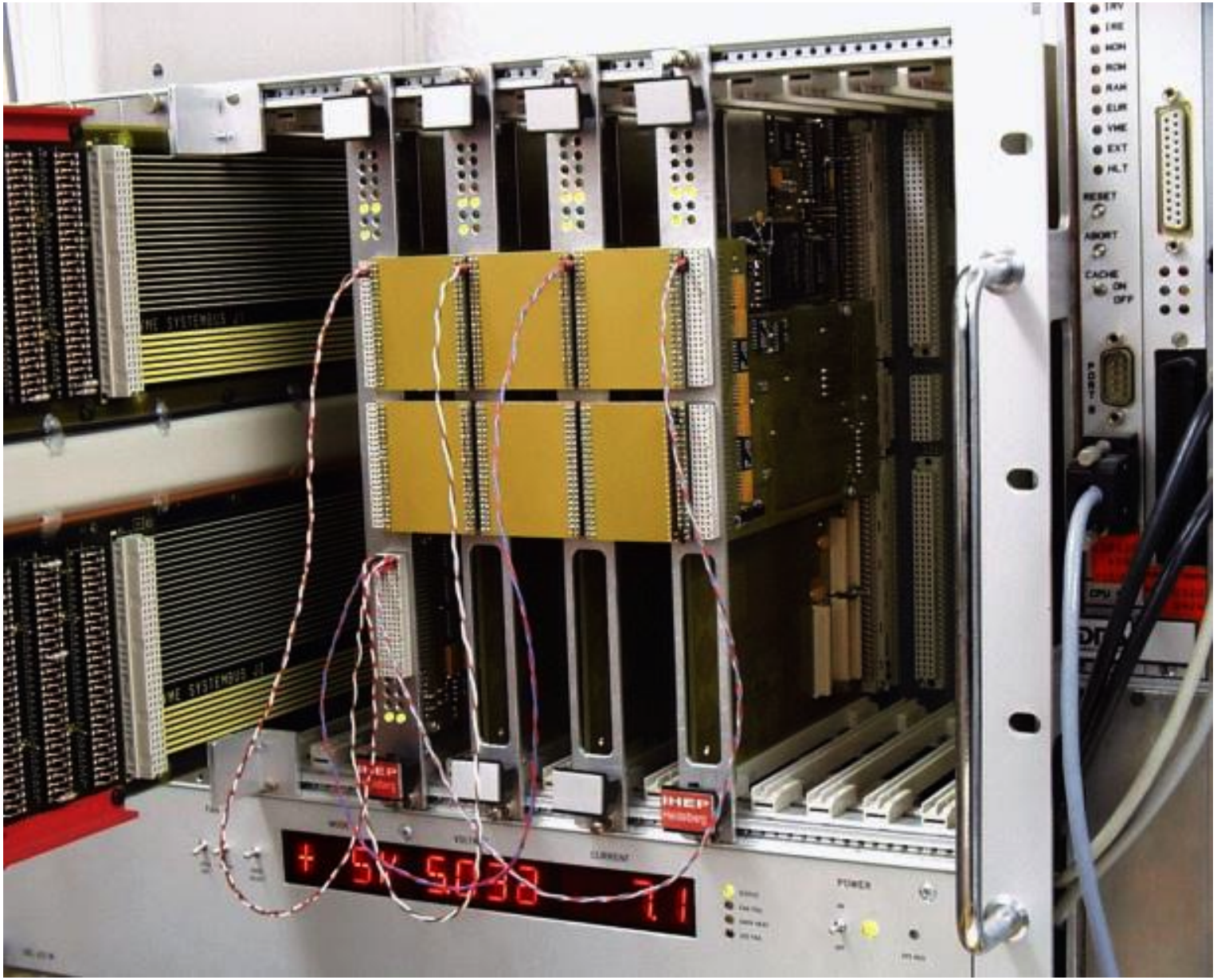
  -> Clock speed of 40 MHz should be possible. -> see figure

The "scalable" PPr Test setup



9u Crate

6u Crate


+ 5V 5.032 7.1
POWER
RESET
ABORT
CACHE
ON
OFF

Material and Misc.

- **Purchase-Summary for the full PPr project:**

  - front-panel connectors (SubD37)
  - VME connectors for PPM boards (J1, J2 , J0-cPCI)
  - cPCI connectors on PPM for LVDS output (B22, B25)
  - "Mezzanine" connectors for AnIn, LVDS "LFan"
  *- ELMA-Trenew: 24 (*8slots)*
  - ReM_FPGA for PPM (XCV1000E)
  - PPrASIC "pre-run"

-->> ca. 30% of TOTAL Heidelberg CoRe spent

- much more to get: PPrASICs/ LVDS-1023s/ MCM-conns/ AnIn PCBs+Comps/ PPM PCBs/ LVDS-drivers PCBs+Comps / VME/ TCMs /PPRODs (... PH's Excel)

••• **"Forget-me-not"s**

- *Cabling: (W.Cleland, SteveH, MurroughL -->> docs.)*
- *Tile-receivers: "electrical" specification to be done for US-team+DOE.*
- *Schedules (PRRs ?) -> see TonyG*

Work Planning (with not a soul too many)

Hardware

- *PPModule*

Following MCM-test including LVDS-CMC (with XCV50E),
define "LVDS_Driver" board with fanout, cable driver + precompensation.
--> Schematics+Layout+Manuf. in Sep./Okt.02 (rm)

Finish-up schematics for MainPPM board (e.g LVDS_Driver)
--> PPM Layout+Manuf. in Okt./Nov.02 (ps)

- *TCM: PPr_Adaptor*

Finish-up schematics; Layout+Manuf. in Aug./Sep.02 (eu)

- *PPROD (9u) after PPM in late02/Jan.03*

Work Planning (cont.)

Tests and Software

- *MCM (incl. ASIC) tests*

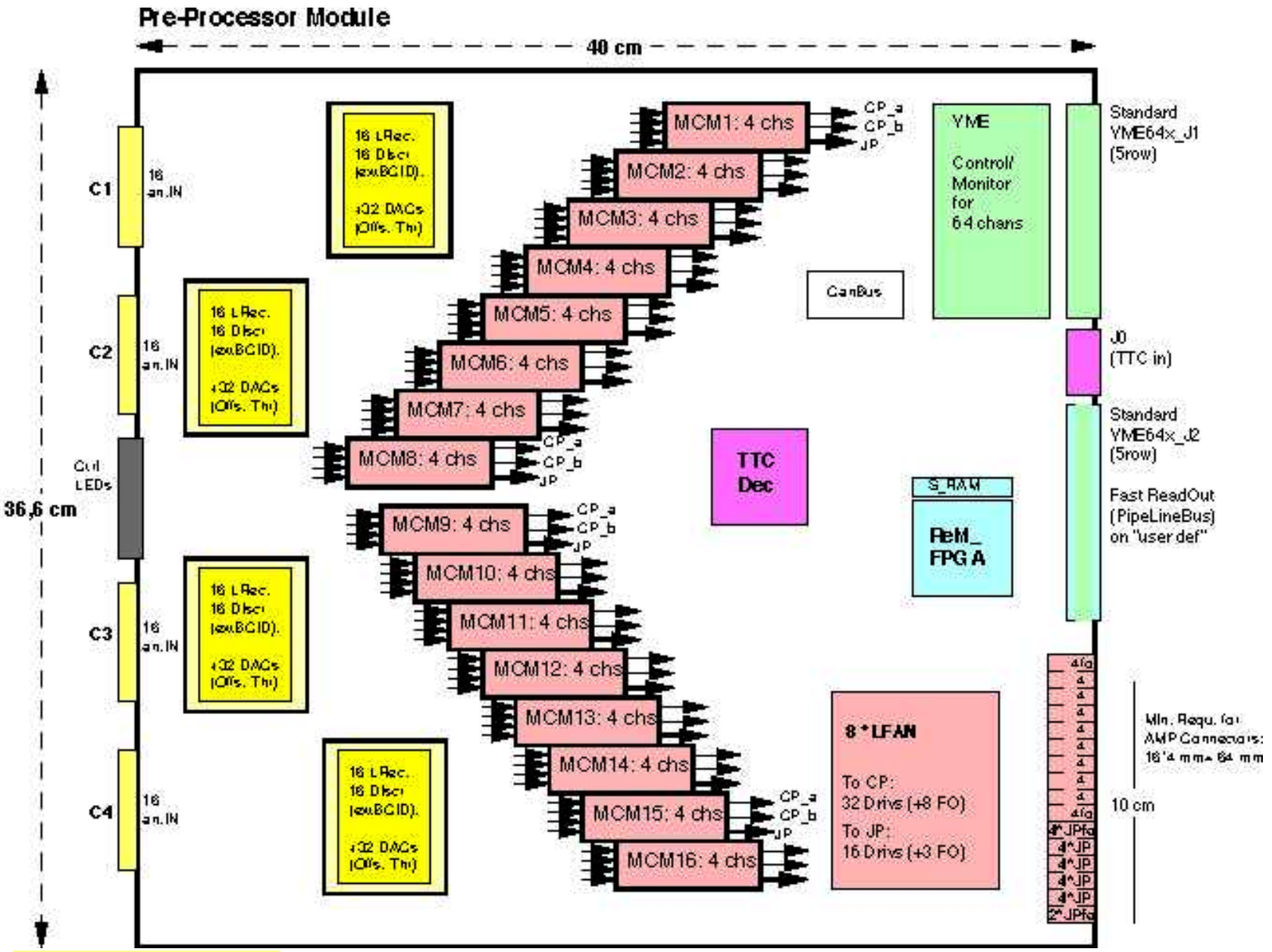
-> ongoing (and maybe finished) till KIP-removal in Sep.02.
-> C-Software to be extended continually from KPenno's work, to run "wafer-probe" test

- *PPr subsystem tests (PPM + VME config. as outlined) in autumn02*

-> include TTCvi,vx in test software... using TCM
-> extend VME test software to PPModule level ...

-> ReM_FPGA code...?.. (compatible with existing pre-ROD ?)

eop


Pre-Processor Module
40 cm
36,6 cm
C1
C2
C3
C4
16 an.IN
16 an.IN
16 an.IN
16 an.IN
16 LRec. 16 Discr (ex.BCID). +32 DACs (Offs. Thr)
16 LRec. 16 Discr (ex.BCID). +32 DACs (Offs. Thr)
16 LRec. 16 Discr (ex.BCID). +32 DACs (Offs. Thr)
16 LRec. 16 Discr (ex.BCID). +32 DACs (Offs. Thr)
Ctrl LEDs
MCM1: 4 chs
MCM2: 4 chs
MCM3: 4 chs
MCM4: 4 chs
MCM5: 4 chs
MCM6: 4 chs
MCM7: 4 chs
MCM8: 4 chs
MCM9: 4 chs
MCM10: 4 chs
MCM11: 4 chs
MCM12: 4 chs
MCM13: 4 chs
MCM14: 4 chs
MCM15: 4 chs
MCM16: 4 chs
CP_a
CP_b
JP
CanBus
TTC Dec
S_RAM
ReM_ FPGA
8 * LFAN
To CP:
32 Drivs (+8 FO)
To JP:
16 Drivs (+3 FO)
VME
Control/ Monitor for 64 chans
Standard VME64x_J1 (5row)
J0 (TTC in)
Standard VME64x_J2 (5row)
Fast ReadOut (PipeLineBus) on "user def"
4fo
4*JPfo
4*JP
Min. Requ. for AMP Connectors: 16*4 mm= 64 mm
10 cm