The Pre-Processor Test Environment

Karsten Penno

KIP, University of Heidelberg

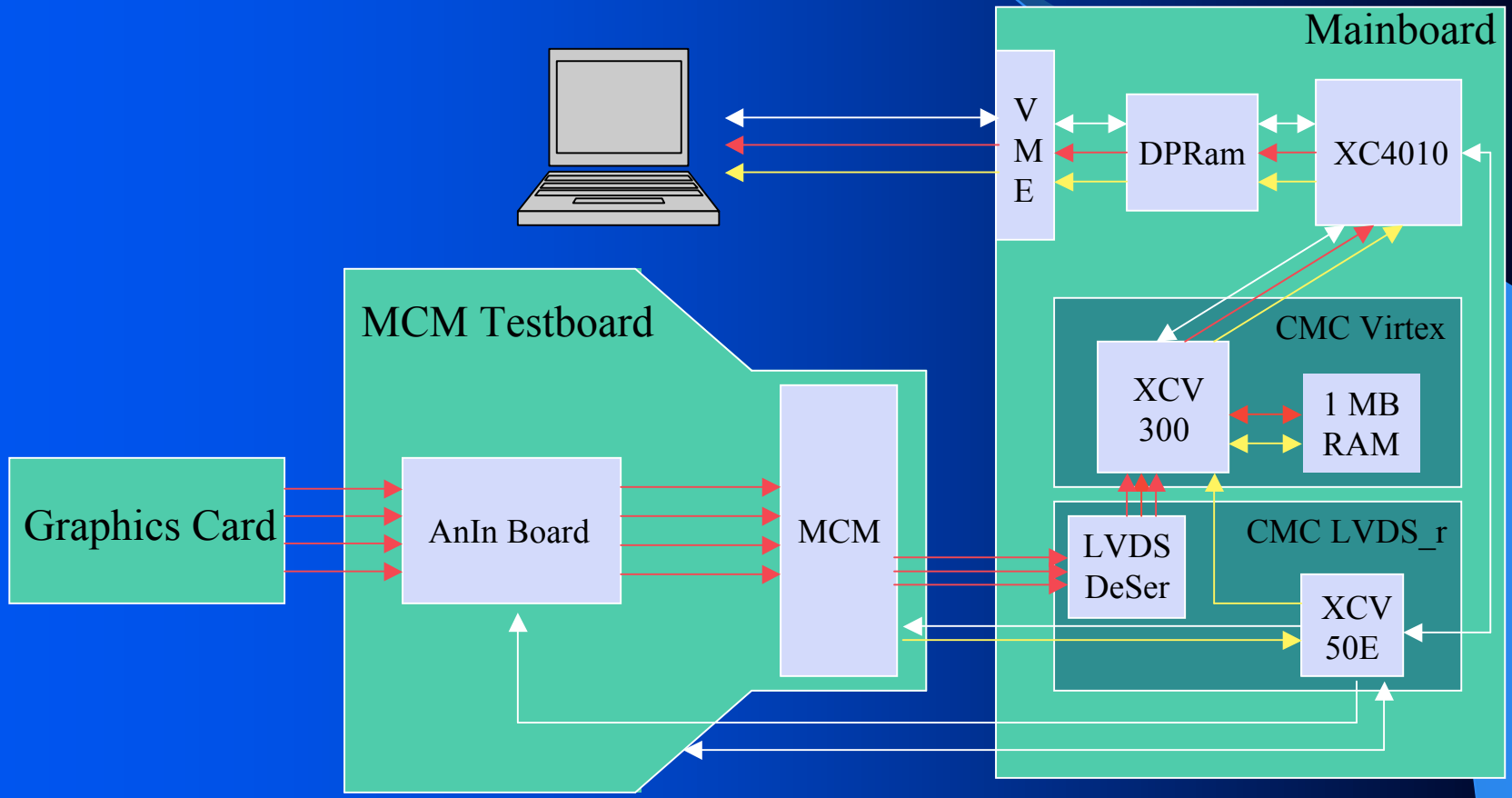
ATLAS Level-1 Calorimeter Trigger Collaboration Meeting

Stockholm, July 4th, 2002

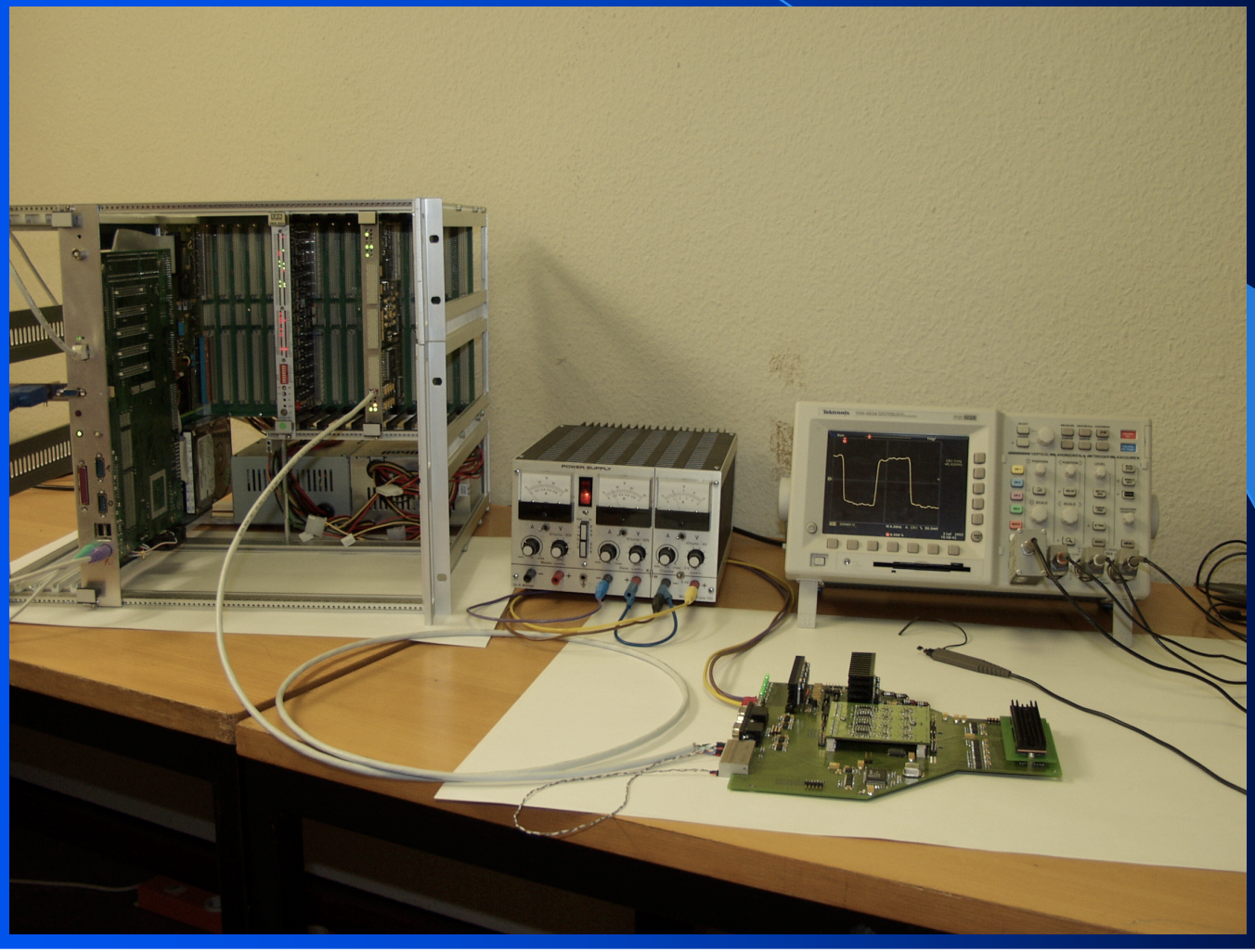
Overview

- Schematic Overview: Data Flow
- Hardware Setup
- First LVDS Results
- Tasks of the FPGAs
- Firmware and Software Overview
- Firmware Status
- Outlook

Schematic Overview



Test Setup



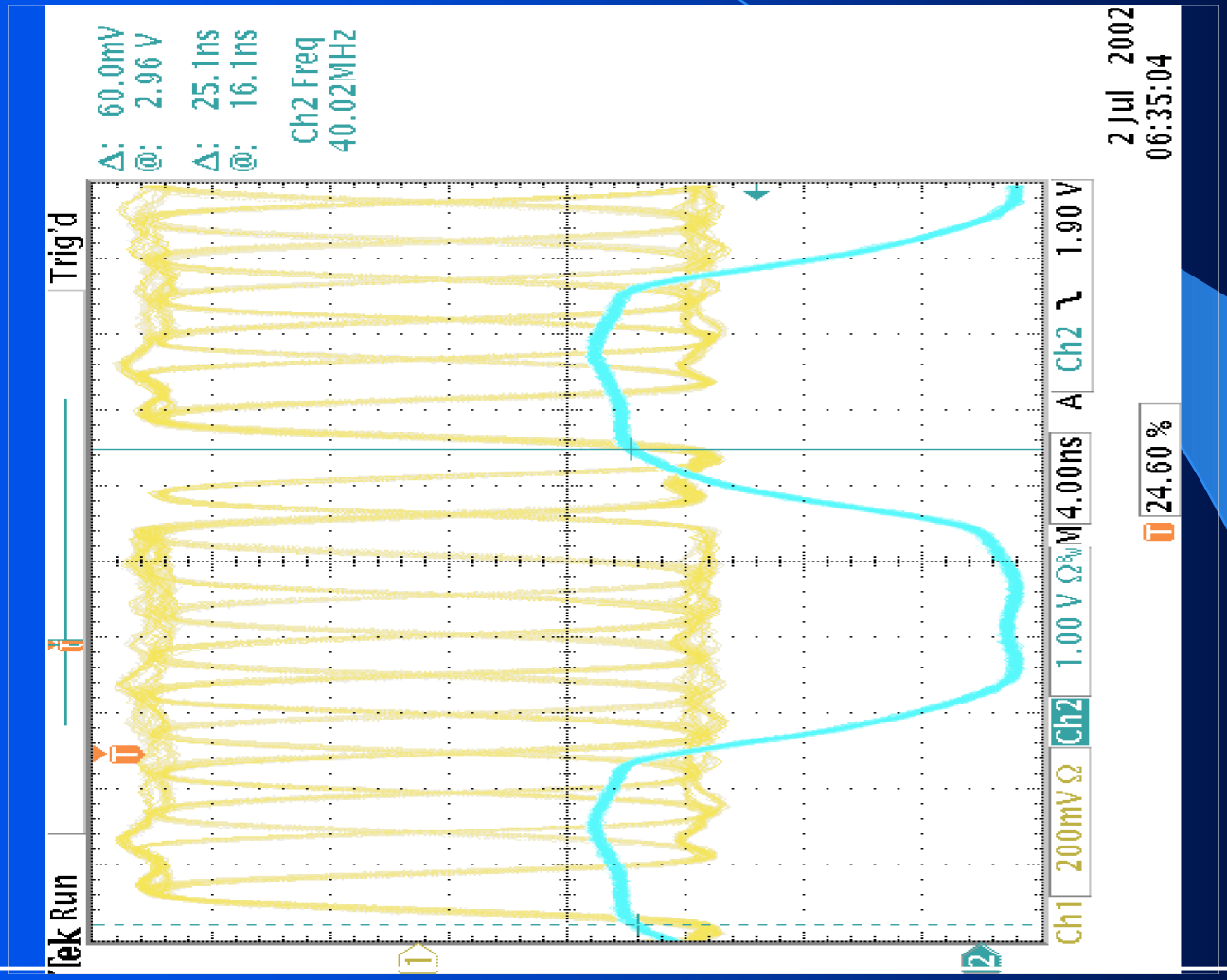
First Attempts of Testing

- No analog inputs to FADCs yet
- No configuration access: rely on hardware default settings
- Initial Test without connection to crate
- Power-Up
- System clock with 40 MHz

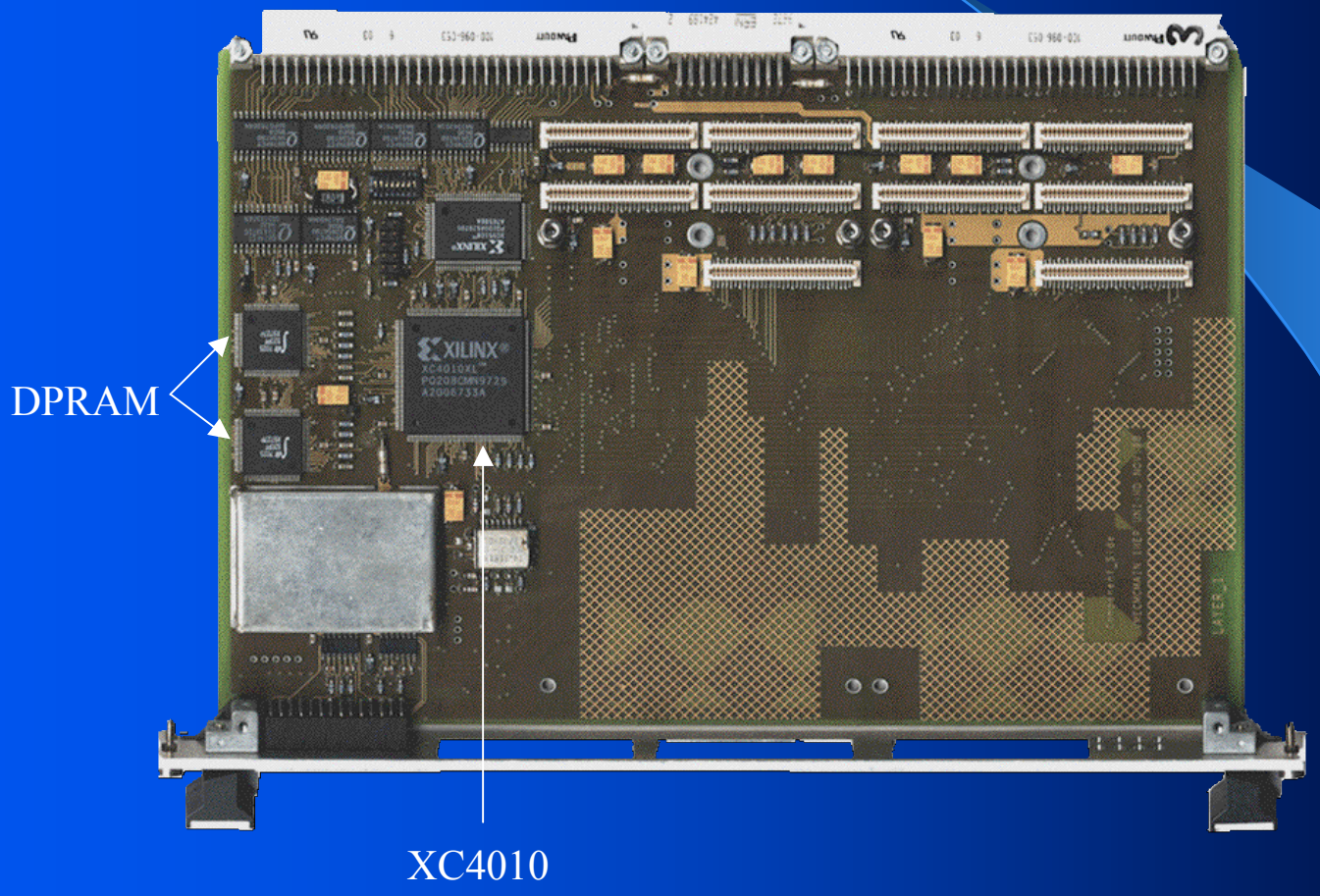
LVDS Results

- Successfully initiated LVDS synchronization pattern from MCM senders
- Observed non-constant LVDS output on all three links (most likely digitized noise from ADC inputs)
- Cable connection: Testboard Crate
- LVDS lock on all three links

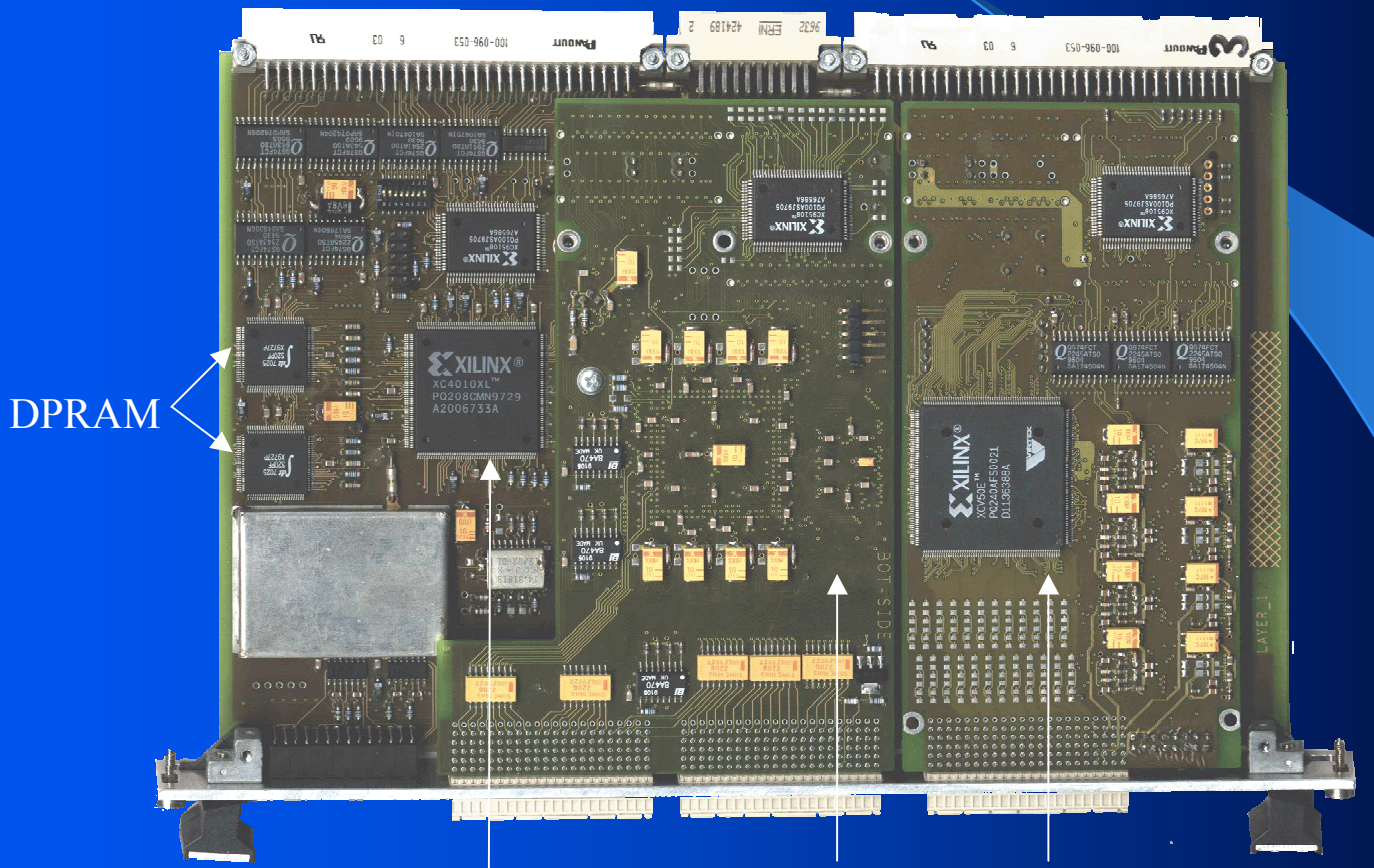
LVDS Data


Δ: 60.0mV
@: 2.96 V
Δ: 25.1ns
@: 16.1ns
Ch2 Freq
40.02MHz
2 Jul 2002
06:35:04
Trig'd
Tek Run
Ch1 200mV Ω
Ch2 1.00 V Ω
M 4.00ns
A Ch2 1.90 V
24.60 %

Mainboard

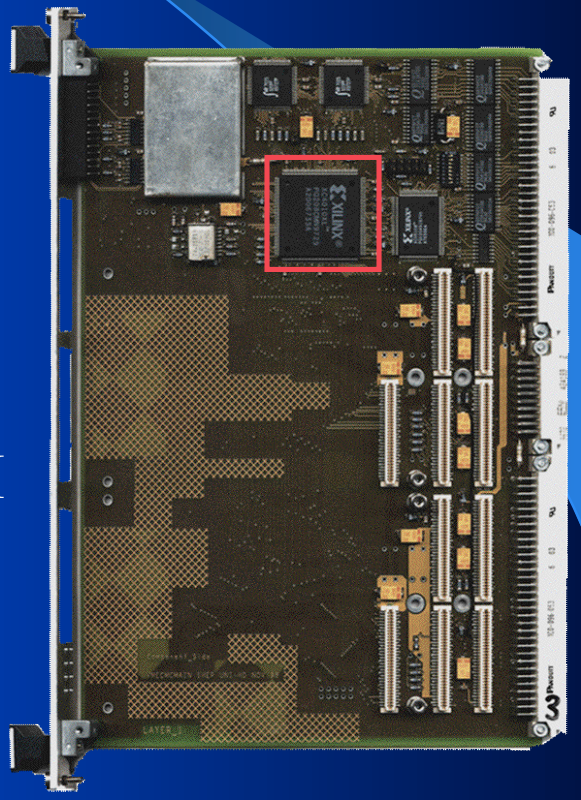


Mainboard

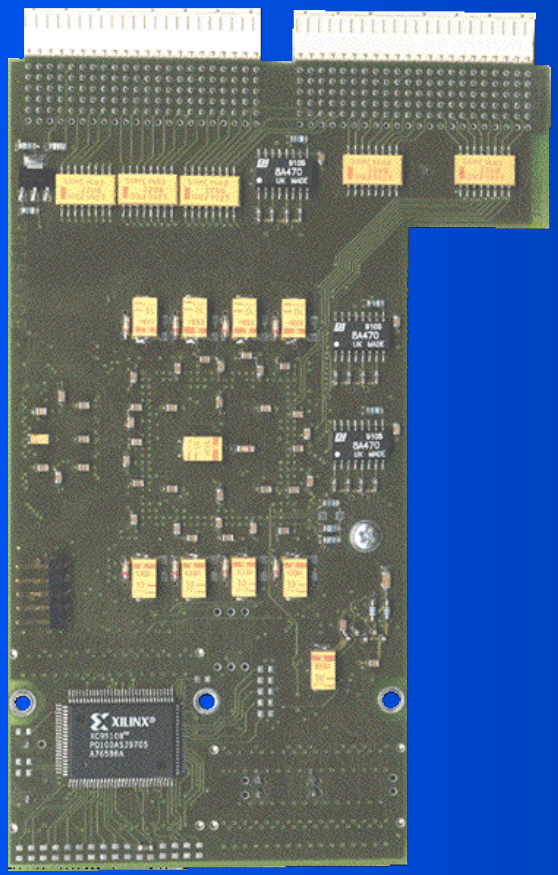


Mainboard FPGA: XC4010

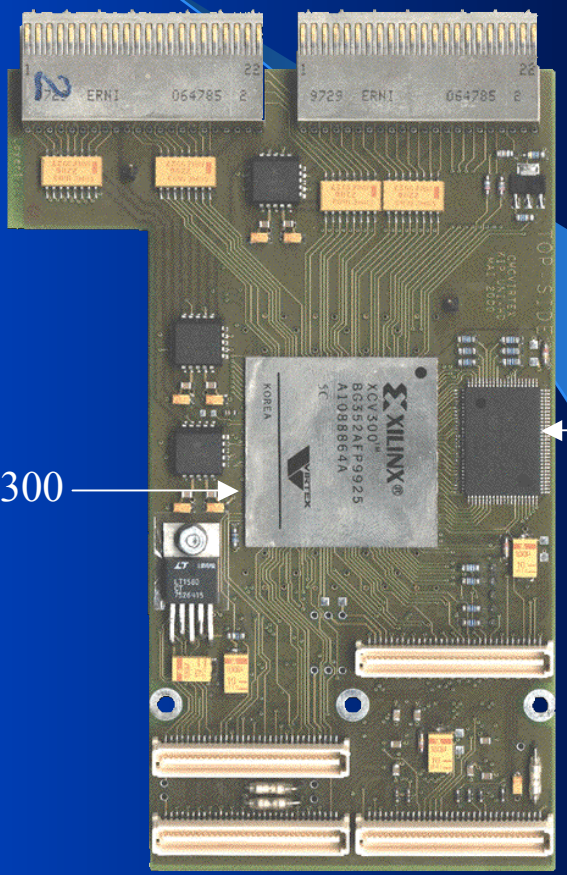
- Interface between VME and test system
- Master: issues commands to daughter board FPGAs
- "Command Processor"
- Sends requested data to DPRAM



Virtex CMC



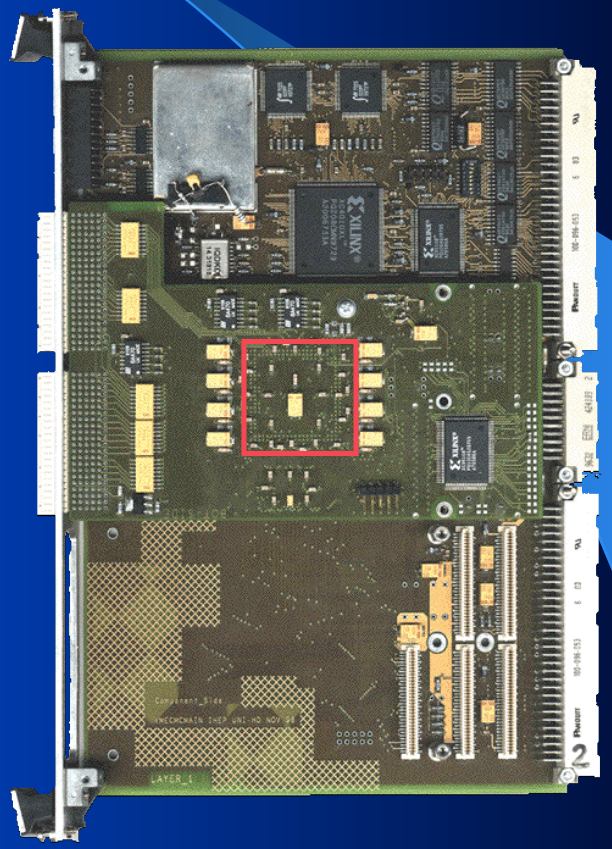
Front



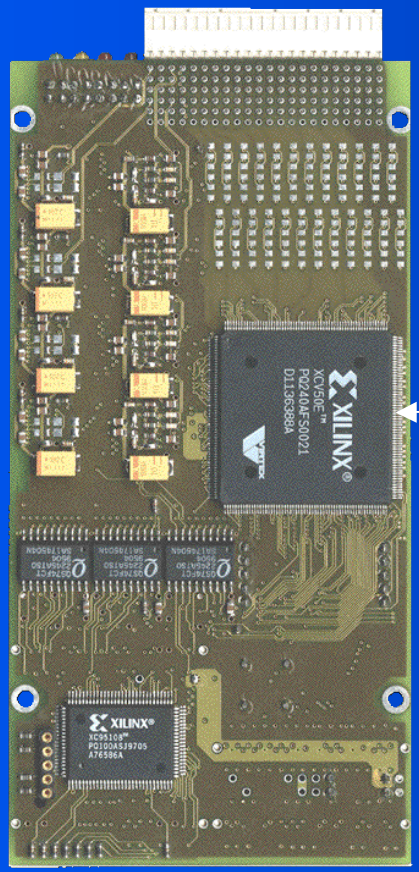
Back

Virtex CMC: XCV300

- Stores incoming real-time and read-back data into SRAM
- Interface between XC4010 and SRAM
- Holds I^2C code

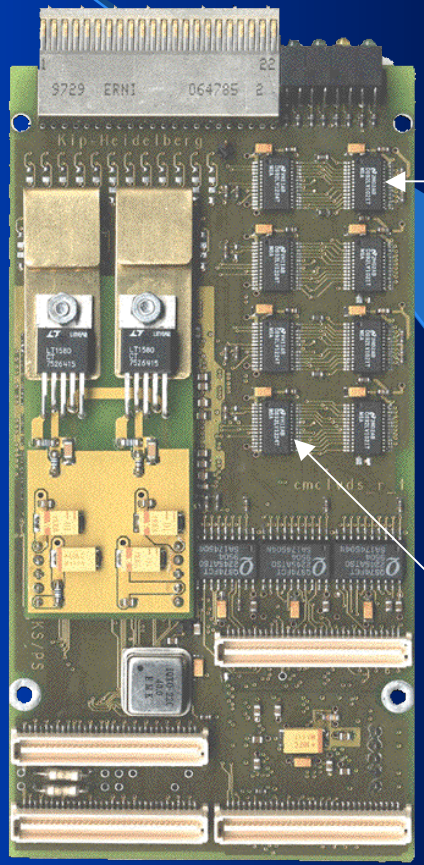


LVDS Receiver CMC



XCV50E

Front



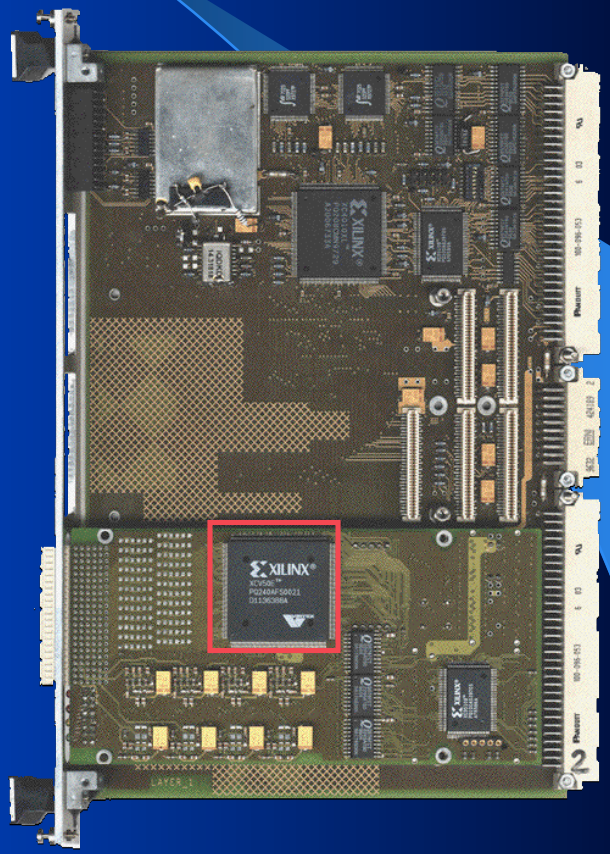
LVDS Ser
(1021),
40 MHz

LVDS DeSer
(1024),
66 MHz

Back

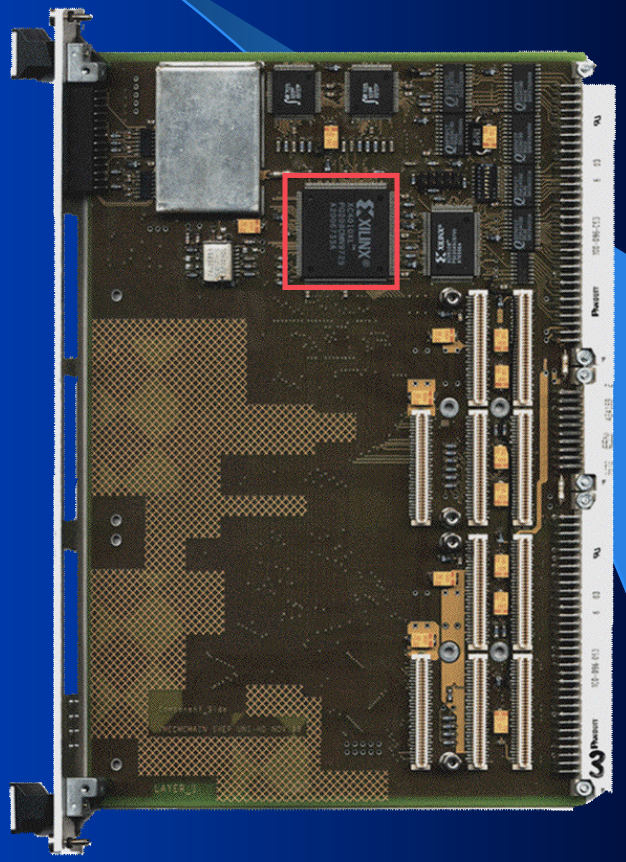
LVDS Receiver CMC: XCV50E

- Handling of differential signals
- Transmits/receives data to/from the serial interfaces of the PPrASIC
- SPI interface for Analog Input Board
- I^2C Master
- Processes I^2C readout data to XC4010



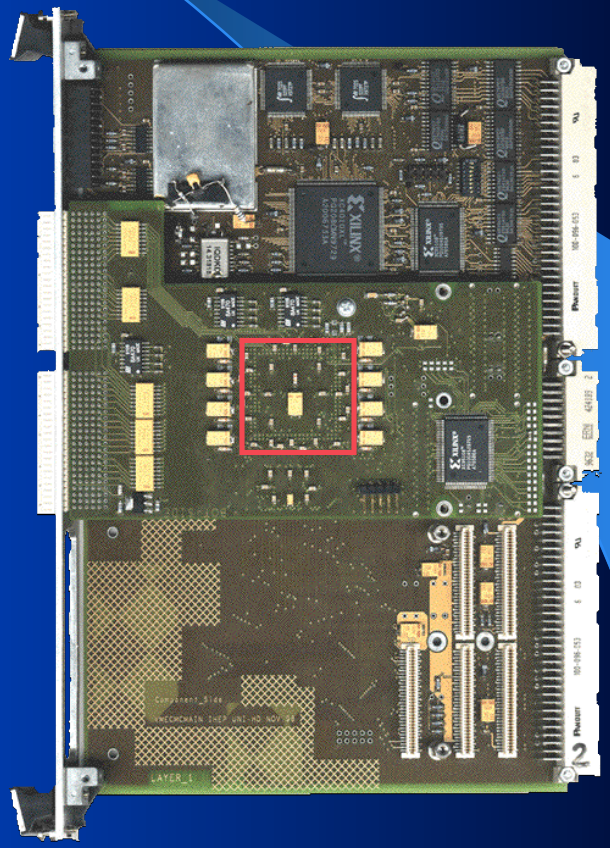
Existing Firmware: XC4010

- Reads command, start address, and block size from dual-ported memory
- Sends subsequent command to daughter boards
- Waits for feedback
- Processes data back to VME



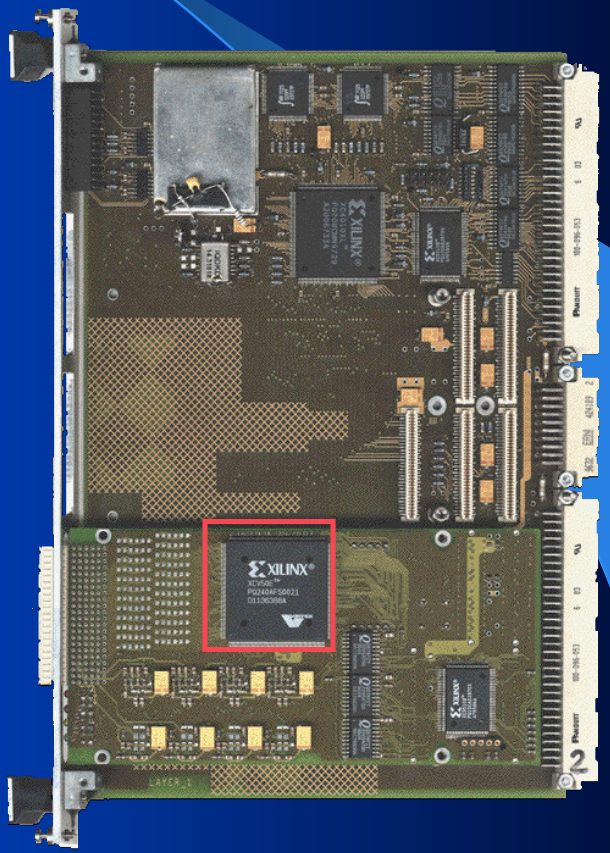
Existing Firmware: XCV300

- Reads data from SRAM and sends it to XC4010 for further readout via VME
- Dual-Handshaked communication with XC4010 (?)
- I^2C -Master Core (www.opencores.org)



Existing Firmware: XCV50E

- Dual-Handshaked communication with XC4010 (?)
- I^2C Master Module currently in XCV300



Existing Software: VME

C++ Program (by O. Nix, K. Schmitt, and K. Penno)

- Sends data words to DPRAM
- Checks for answer from the XC4010 (command acknowledge)
- Checks start address
- Polls for terminating signal from XC4010
- Writes data into a "Root" file for further analysis

Firmware Status

- XCV4010: almost ready
- XCV300: still problems with handshaked communication
- XCV50E: serial interface and other control I/O has to be implemented

Outlook

- Completing FPGA firmware
- Analog Input:
  - "primitive" pulses
  - pulses generated by graphics card
- Interpretation of LVDS data