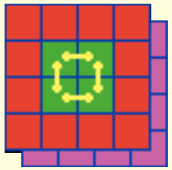


White nights and dark nights: Stockholm, 4–6 July 2002

- Personal view, not a comprehensive summary of all that was presented and discussed.
- Apologies for anything important that's missed — tell me.
- If you think anything is mistaken or objectionable please say so!

- Categories are as follows:

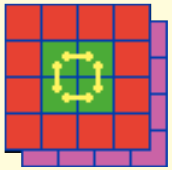
  +□A (mainly) positive development, or something that has been sorted out, or simply good progress.

  –□A negative development, or something that needs to be sorted out that may cause problems, or an item where work seems to have stopped — no criticism of people involved is (necessarily) implied.

  ◆□More work or a decision is needed.

  !□A controversial point that must be discussed further.

- No names mentioned since it's very difficult to be fair to everyone who has done all the work — people will know who they are!



Physics simulation

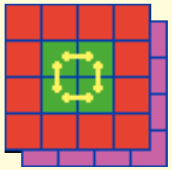
+ Work continues to progress on offline trigger simulation
+ Jet trigger ~ done, energy triggers soon

– Who carries on the work long-term?

◆ Must validate by duplicating TDR plots; then use new detector description
◆ Later add features such as thresholds varying with location
◆ Must add an 'analogue' simulation, such as noise added en route to the trigger and time history of pulses

+ Simulation of jet processing on JEM underway

◆ Make sure FPGAs have sufficient spare capacity to allow for future changes, e.g. dedicated secondary RoIs



Calorimeter signals and cables

+ Pittsburgh will build LAr receivers

+ Nice idea to combine muon and calo TileCal signals, allows use of LAr-type cables, saves on total number of cables, etc. DO IT! But note that cable impedance is 90Ω!

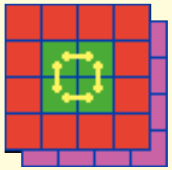
+ Good progress made on documenting input connectivity

– Pittsburgh offer to build TileCal receivers still not formally approved

◆ Must write specifications for TileCal receivers (also said this last time)

◆ Finish documenting connections from calorimeters to Preprocessor, and check them

◆ Grounding in combined cables?

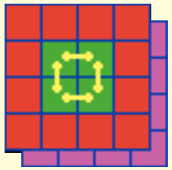


Preprocessor

+ ASIC now mounted on MCM, and testing of both is now starting; lots of work done to prepare for a thorough job of testing both ASIC and MCM
+ Plans to test AnIn and LVDS daughter cards soon

– REM FPGA firmware must be made to fit in FPGA, and not clear who will take it over
– PPM and ROD late; problems if they slip any further
– Effort not presently available to work on test and simulation software within our online framework; not clear what will be available for subsystem and slice tests

◆ Must show that Xilinx is a good LVDS fanout choice



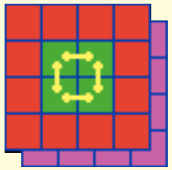
CPM and JEM

+ CPM has arrived and is being tested; so far so good
+ General comment *(not just CPM!)*: We have now shown that we can build 9U modules with dense connections and big BGA FPGAs!
+ Realtime data path on JEM-0 being tested (a bit slowly; TTC would help)
+ Work on JEM firmware is progressing, both for jets and energy triggers
+ Nice work done on jet algorithm

– JEM design iteration to full specification for slice tests planned, but will take time

◆ Must test JEM-0 with backplane soon
◆ Test plan for JEP subsystem must include tests module-to-module and with CMM and ROD before slice test

! JEM iteration makes logical changes in chip families, but taken together the changes are not trivial
! Must be sure to optimise cooperation between Stockholm and Mainz



Common modules and backplane

+ CMM has arrived and is being tested; so far so good
+ Backplane has arrived and is in use; very few problems found

– Crate mechanics a bit marginal (final solution will be better)

+ TCM, adapter link card and VMM all in use
+ Further progress on debugging and firmware for CP/JEP ROD prototype; also improvements to DSS including GIO card and proper handling of L1A

◆ Still need several other CMM and ROD firmware versions

DCS, calibration and joint tests

+ CANbus ADC readout and communication on backplane now working
+ Fujitsu now looks like the feasible, compact and cheap solution we hoped for

+ Proposal for very useful work (some in test beam) with calorimeters and other parts of T/DAQ in 2004
+ Limited work with calorimeters in 2003

– Beware of overcommitment w.r.t. slice test

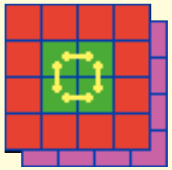
! Microcontroller per module allows later decision on how elaborate monitoring system is

! Should we try to monitor FPGA *current*, to catch mis-configuration?

◆ Design DCS monitoring to minimise amount of software effort needed, since it is in short supply

◆ Finish document on our calibration requirements; continue to liaise with calorimeter calibration people

◆ Must be organised to minimise unnecessary effort and factor out what really needs actual beams



Online software

+ Much progress on module services, databases, run control, individual modules, test vectors, Linux systems, ... towards slice-test environment
+ Scheme for running tests being worked on

– Big shortage of effort on the software, and this is now delaying some hardware testing!
– Concern over long-term development and maintenance of HDMC

! Try to get non-software experts to do as much module testing as possible (also said this last three times)

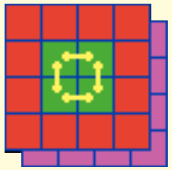
◆ Need to work on test vectors for larger, diverse subsystems
◆ Need work on event and hardware monitoring
◆ Must talk more to CTP and the rest of level-1

Tests and timescales

+ Modules and ASICs have now appeared; a great deal has been achieved and the 'landscape' now seems very different!
+ New and detailed schedule; largely based on having real hardware

– Individual and subsystem test phases are complex and it is very difficult to predict duration (also said this last three times)
– Caution: slice test now in spring, was autumn at last meeting and previous spring the one before!

◆ Must not send modules for slice test until they are working well on their own *and* in their own subsystem (also said this last two times)
◆ Must adapt FDR/PRR review process to be useful but not excessively heavy
◆ Agree milestone list, consistent with detector availability, by end of summer



Summary

+ People are being very open about problems as well as successes

+ There has been a lot of progress, and much hardware now exists. Very exciting period underway!

– ... But also more slips in timescale, and worrying shortage of effort (also said this last two times)

Thank you to the Stockholm group for a productive, well-organised meeting *(and dinner)* in lovely surroundings!

Belated best wishes in your handsome new building!