Timing Control Module *(TCM)*

VME Mount Module *(VMM)*

General-purpose I/O Card *(GIO)*

Status

Timing Control Module

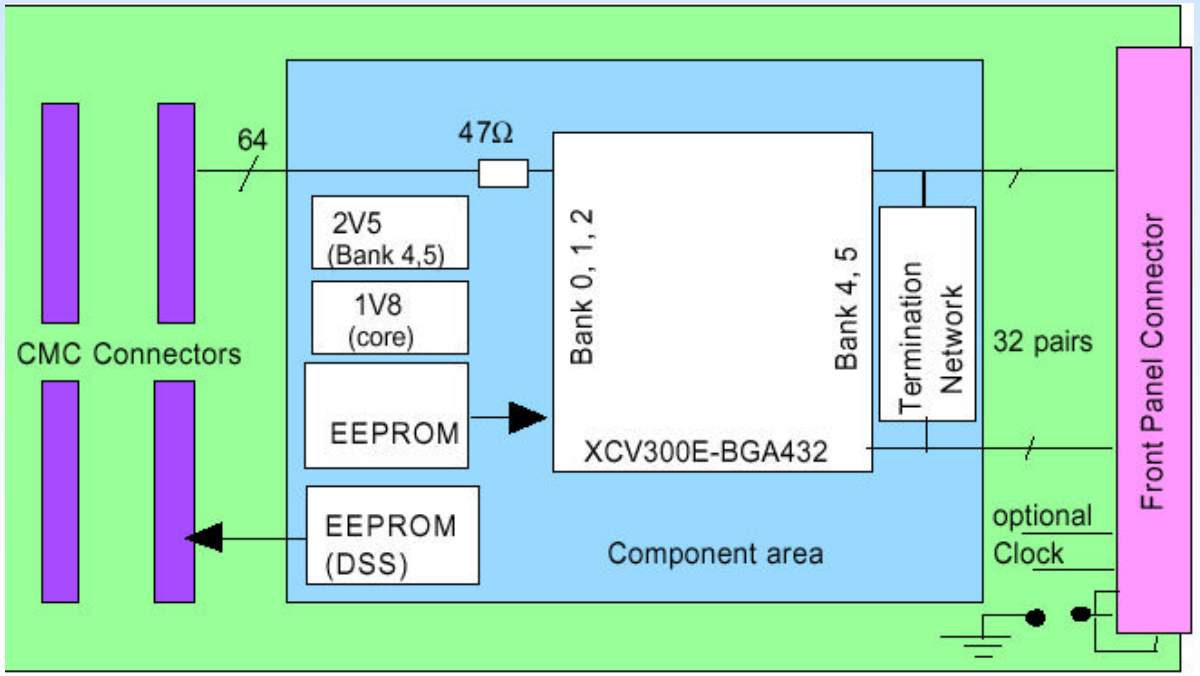
- **TCMs in Birmingham *(CPM tests)*, RAL *(CMM/CANbus tests)* and Heidelberg *(adapter card needed for VME64x crate/backplane – PPM tests)***
- **Small design problem recently discovered with front-panel VME display function:**
  - **Fails to display VME data latched by other modules in same crate – OK for its own data**
  - **Solution will involve a CPLD firmware update and a small hardware modification**
  - **When checked, documentation will be updated and new CPLD files issued to all users *(Birmingham, Heidelberg and RAL groups)***

VME Mount Module

- Two VMMs now in operation with Concurrent processors – in Birmingham *(CPM tests)* and RAL *(CMM tests)*
- Problems *(none serious)*:
  - Front-panel RESET mode selectable – but selected mode not clearly indicated
    - *Bricollage* solution at present – will be fixed properly in next (production) version
  - Capability to set Crate Geographical Address could cause contention with GA setting from the crate itself
    - This feature is now disabled – crate alone sets its GA
  - Front-panel Geographical Address LED display shows complement of GA!
    - Still to be explained …
  - Incorrect VME connectors fitted originally
    - To fit correct connectors requires slight mechanical modifications to the pcb

General-purpose I/O Card

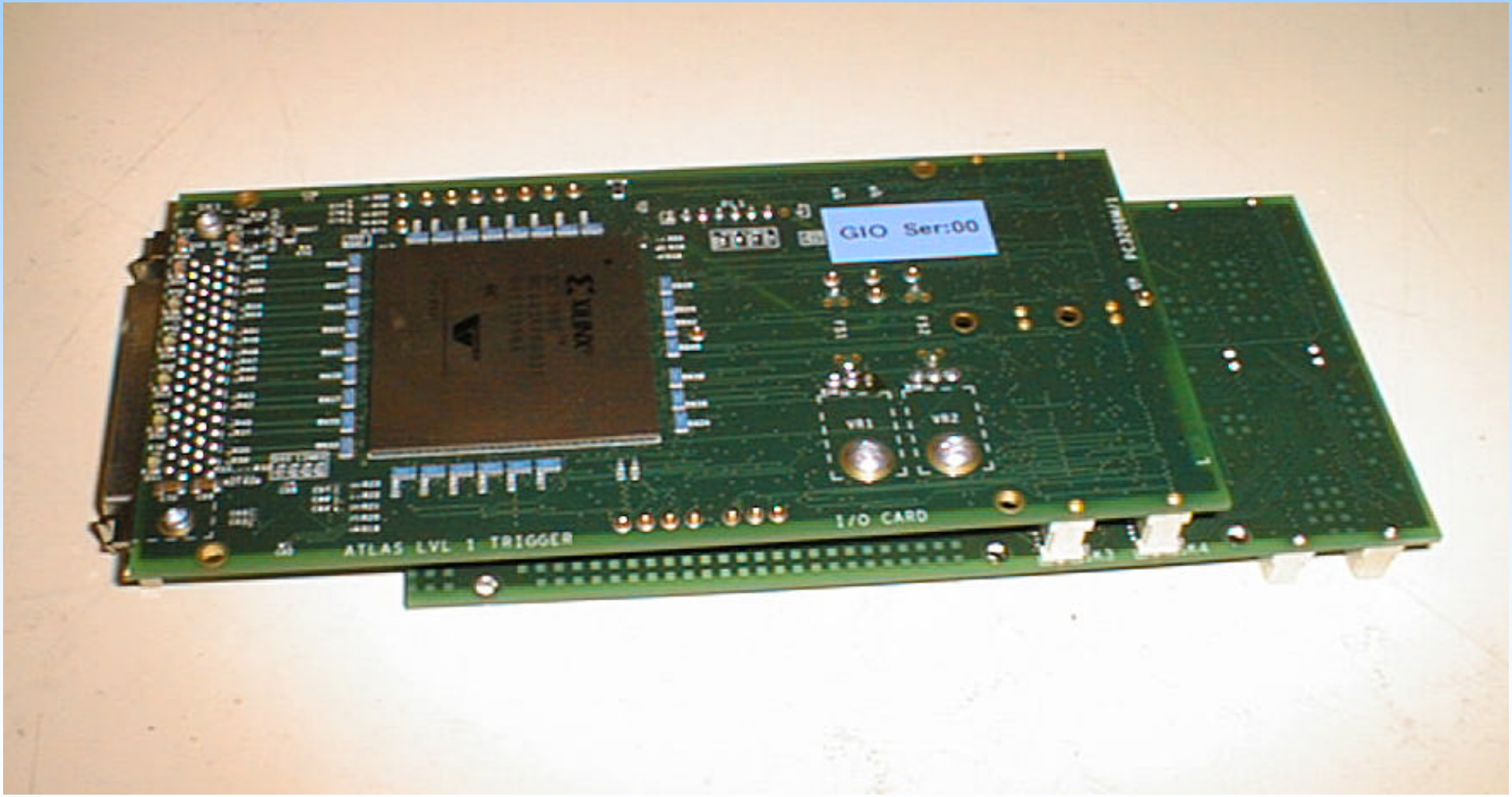
- DSS-mounted Tx/Rx emulator CMC card – for testing CPM, CMM, JEM, …
- 32 LVDS data I/O pairs + clock *(or 66 single-ended signals)*
- Can provide other I/O standards – LVCMOS, PECL, …
- Design based on Xilinx XCV300E Virtex-E FPGA
- JTAG port for FPGA access and ISP



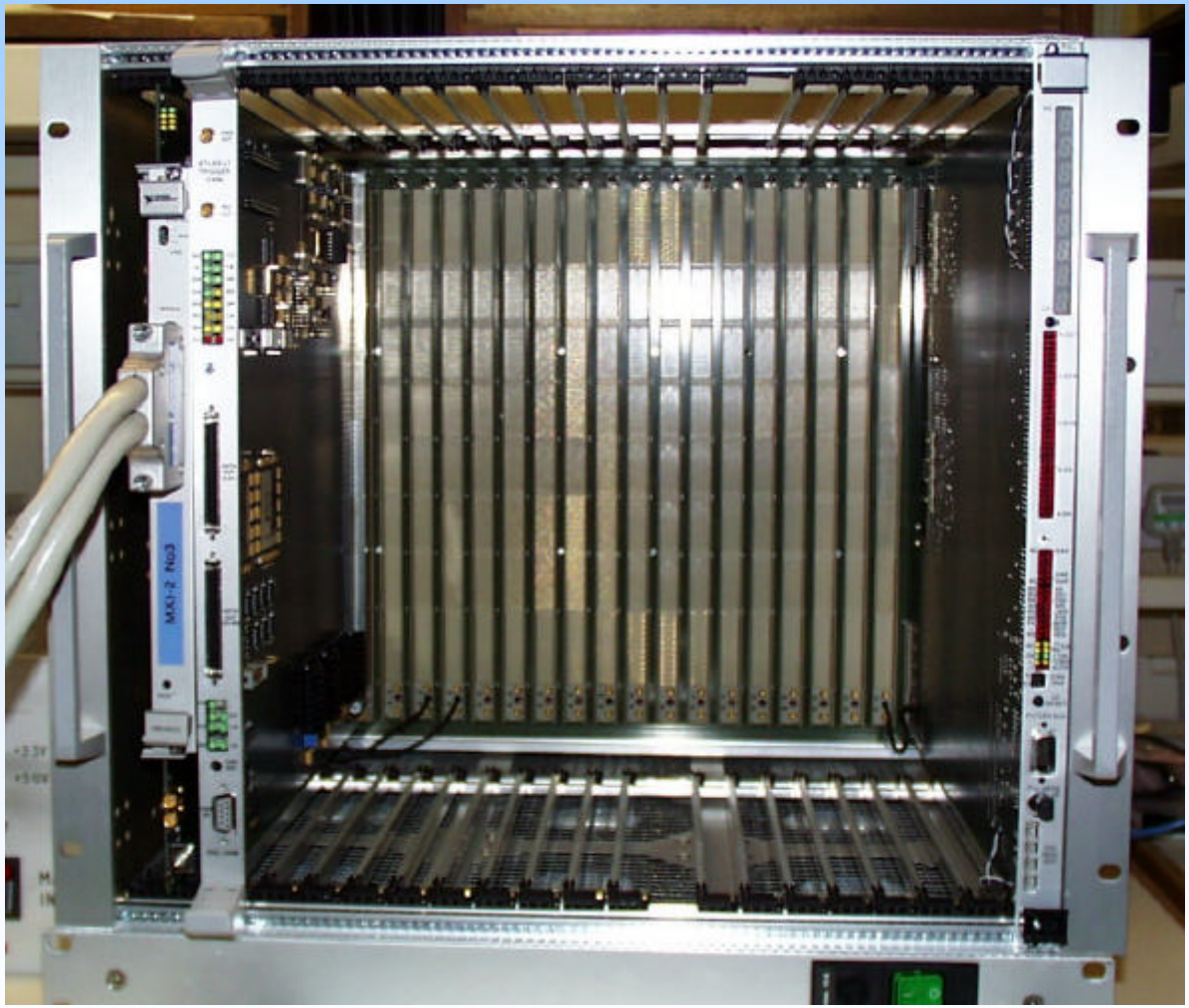
General-purpose I/O Card

- Two cards assembled and under test
- Layout problem discovered:
  - CMC connectors – placement rotated by 180 degrees
    - *Bricollage* solution at present – Interposer adapter card to re-map pins ←→ DSS motherboard connectors to allow testing
    - Will be fixed properly in next iteration
- Card powers up on DSS motherboard OK
- JTAG chain established
- PROMs programmed
- FPGAs configured
- Testing continuing …

General-purpose I/O Card



CANbus Tests



- TCM-CMM CAN dialogue successfully established *via* crate backplane