ATLAS HEC: TOWER DRIVER BOARD

(TECH. DESIGN REVIEW, 13.JUN.02 @ CERN)

Summary of ph:

1. Rad.hard Voltage regulators shall be used to get from +/- 7 V (picked up from FrontEndCrate's power-rail) to +/- 5 Volt supplies on board. It is understood, that the design/fabrication of the negative regulator meets obstacles currently. Given the total consumption of the TDB, the use of a rad.hard commercial (less current) alternative (from Intersil) should be investigated.

2. Allocation of power-rails (which voltage/ampereage where) in the FEC shall be coordinated among all board designers.

3. Water-flooded cooling plates don't seem to be necessary for the TDB (it consumes 13 Watt only). However, the heat-unloading onto neighboring boards should be agreed on within the FEC.

4. 50 Ohm termination at TDB input looks in several respects better than the series-resistor at LSB-output only with high-impedance input at the TDB. Hence, it was recommended to implement 50 Ohm at the TDB input and compensate by double gain.

5. The "grounding configuration" at the output, i.e. cable-transmission to USA15 barrack shall be made "uniform" for all LAr. In particular, referencing of "pair-shields" and "global cable shields" shall be equal in EmCAL and HEC as well as conforming to the ATLAS "grounding rules".

6. The "saturation point" in the analog signal chain of HEC is different from the other LAr calorimeters. It lies in the "Lin.Mixer/ LayerSummingBoard combination", whereas the EmCAL saturates in the "TowerBuilder" (last stage). The TowerDriver is "neutral" (quotation). It should be made sure, that electronic saturation behaviour is equal to the EmCAL.

7. Addition/Removal of the fourth layer is a software-controllable option, which can be changed at run-time.

8. Fusing individual PCBs is recommended to keep crate-wide power-supplies operational, if a local fault occurs.

ATLAS EMCAL: TOWER BUILDER BOARD

(TECH. DESIGN REVIEW, 13.JUN.02 @ CERN)

Summary of ph:

1. Presentations on the TBB revealed, that the maximum point of good linearity is moved to 3.0 Volt (representing 256 GeV Et). This was never requested by the trigger, which asked for 2.5 V corresponding to 256 GeV Et. The 3 Volt range in the analog chain is the headroom to be readjusted to 2.5 V in the Receiver-system and to ensure clean clipping in the FADCs. However, if required by supply-voltages (+/- 6V instead of +/- 7V in FEC), the end-point of good linearity could be moved down to 2.5V in "earlier" parts of the chain (e.g. the TowerBuilder).

2. Discussion showed, that "sensitivity/gap" [muAmps / GeV] has not been verified since the early days of the EmCAL. A calibration run on a module should verify the "old" calculated values. Sensivity should be uniform along tower-depth – or gain-adjustments should be adapted - such, that the TBB adds-up true energy in its analog summation.

3. Power-handling on-board is done by fuses and ohmic drop across resistors. While fusing is desirable (see 8. on HEC-TDB), regulators for power-adjustment should be used (see 1. on HEC-TDB).

4. There is digital control-logic present on the board (e.g. setting of delay-lines ...). While this is usually quiescent during data-taking, some slow-control components (DCU2) require a permanent 40 MHz clock for digitizing analog levels. Hence, possible influence of "digital noise" on analog signals should be checked thoroughly on the final PCB-layout.

5. Saturation in the TBB looks well controlled, i.e. pulses for very high Et are decreased in amplitude, BUT never fall below the 256 GeV-equivalent !!

6. It was suggested, that noise should not only be measured in the frequency-domain (spectrum-analyser with 10 MHz limit), but also in the time-domain with a high-bandwidth scope. The scope-RMS shall be compared to the frequency-integral.

7. Timing of layers (by delay-lines in the TBB) for good, linear superposition can only be verified by digitisation in the Pre-Processor's FADCs. The Review-Chairman declares this for obvious reasons to be a COMMON procedure between LAr and Level-1.

8. J.Pascual informed, that the "long" cables from detector to USA15 have 90 Ohm impedance. This was chosen by Saclay for reasons of propagation-time (latency). PH takes note of this and informs Level-1.

9. Noise above 10 MHz is "unknown territory" to date. Filtering for highest frequencies is foreseen down-stream (Receiver, Pre-Processor), but noise intensities shall only be known when noise of the entire chain within a FEC can be looked at.

10. Signal distortions due to impedance jumps in cryostat-cabling are present on the trailing edge of the signal. They move from behind the peak all the way down to the end-of-pulse depending on ETA. Their influence on the pulse-integral (FADC-output and FIR filter) is small (few percent), hence, can be corrected in the PPr-LUT.

11. TBB-Input termination by 50 Ohm (see 4. on HEC-TDB) shall be foreseen.

12. A responsible person for configuration of all PCBs in the FrontEndCrate shall be nominated. Somebody from Saclay could be a logical choice.