Jet/Energy Module
-status of prototype tests and firmware-

ATLAS Level-1 Calorimeter Trigger Meeting

Stockholm, 4.7 - 7.7.2002

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STATUS REPORT
- JEM0.0 Tests and Firmware -

- JEM0.0 : test results
  - RTDP (real time data path) => current status
    - LVDS Links & Input FPGA
    - Interface : Input FPGA ⇔ MainProcessor
    - MainProcessor
- Firmware status
  - Changes of existing firmware
  - ROC (readout - controller)
- Test vectors for JEM0.0 prototype
- Outlook

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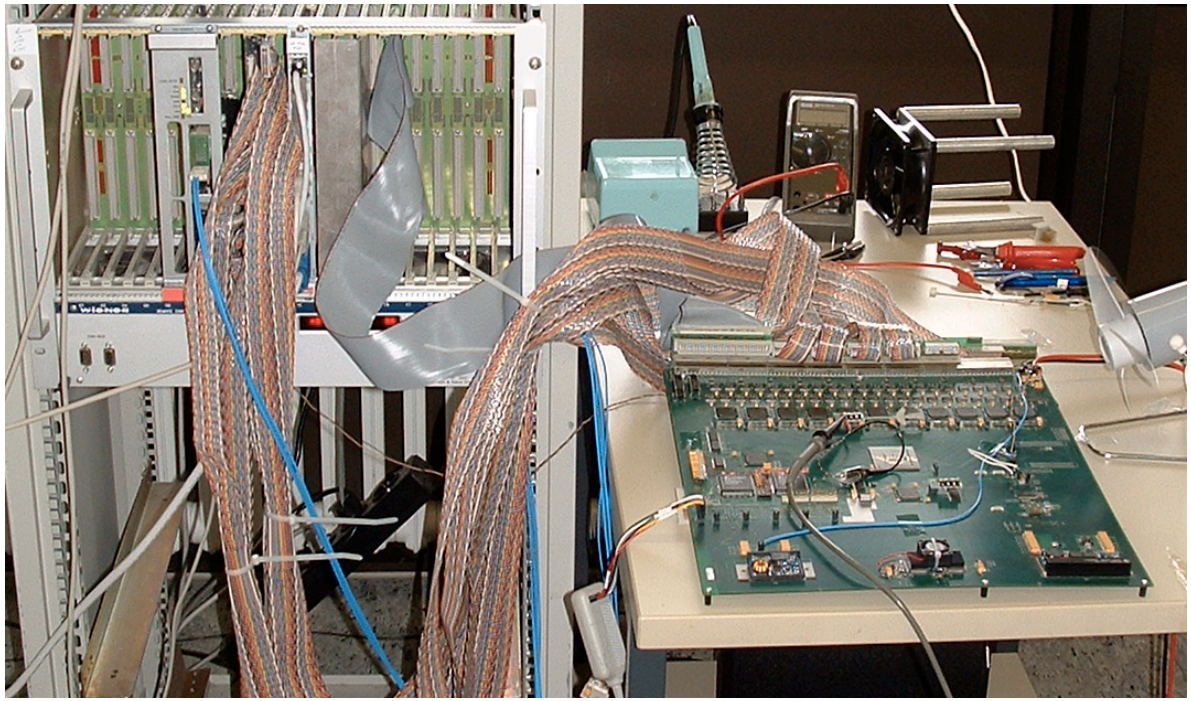
JEM0.0
Test Set-up in Mainz

- JEM0.0
- DSS Module with LVDS Source Cards
- Link-Replicator-Module
- Crate-CPU with Linux and HDMC
- („high end“) Oscilloscope



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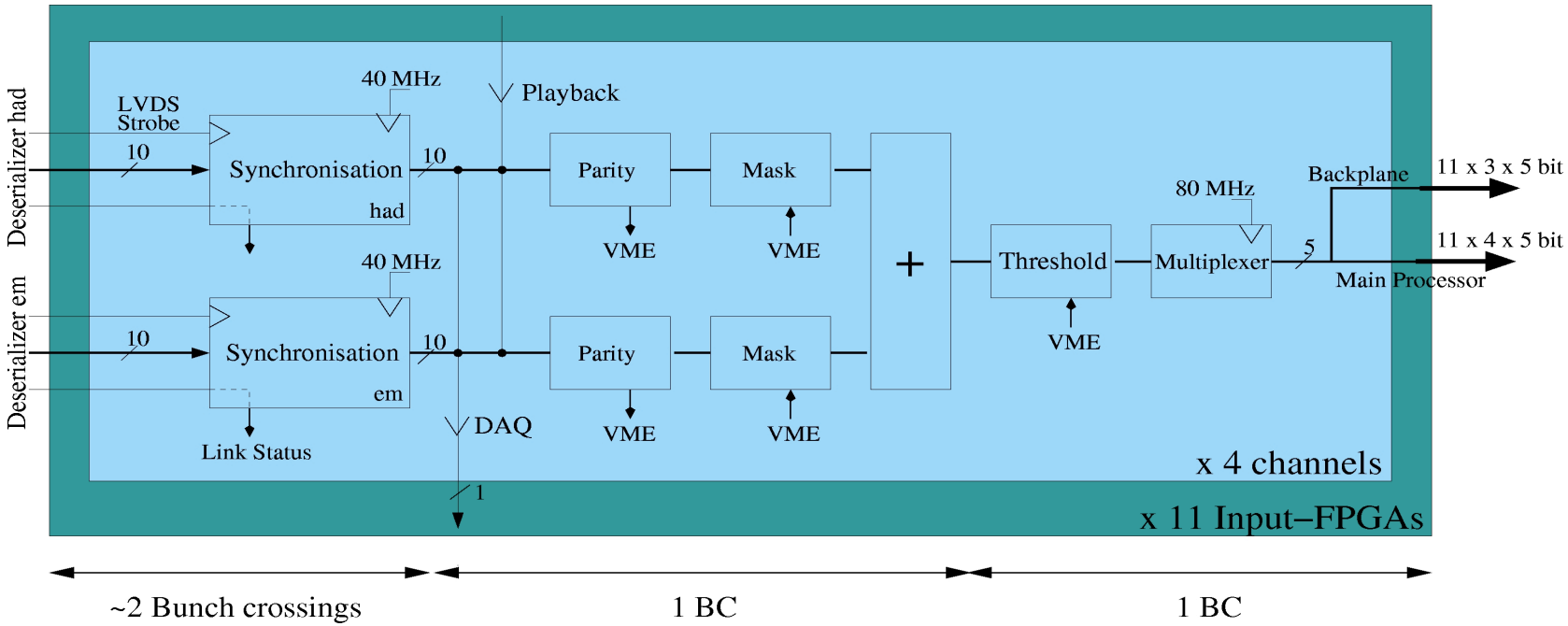
„Recap“

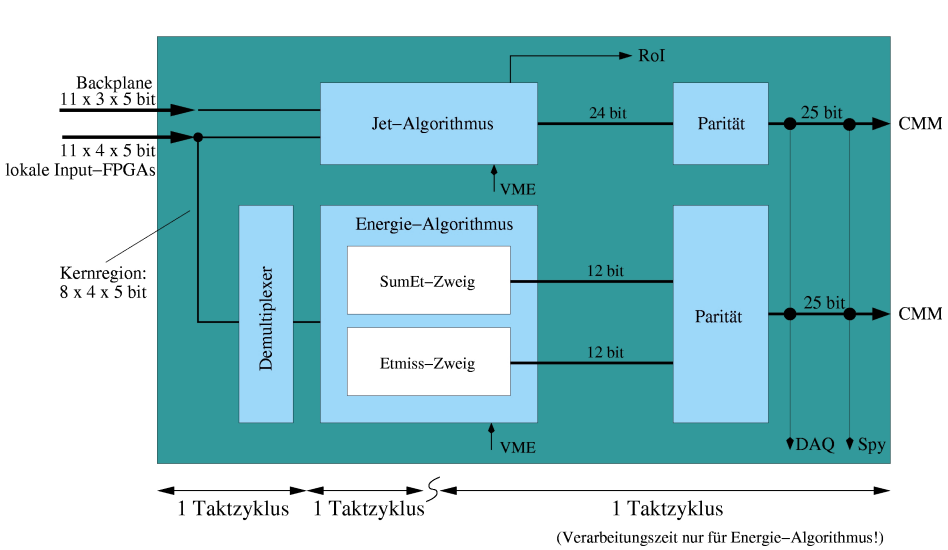
RTDP implementation (InputFPGA)

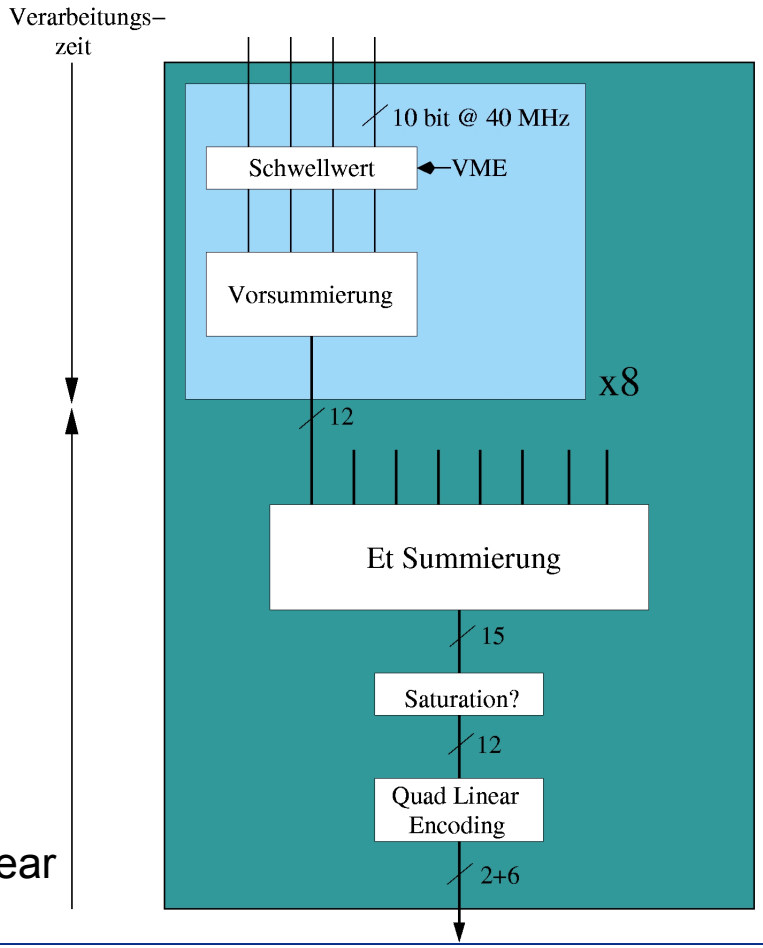


Test results:

all functionalities of implemented code except synchronisation (0° phase fix) and playback memory were tested successfully

„Recap“
RTDP implementation (MainProcessor)





Important for tests:

- spy memory (depth: 256 slices)
- signal and read back only possible via VME due to software issues
- incoming data after de-multiplexing are captured (--only for test purposes) and E_T-Sum is after quad linear encoding

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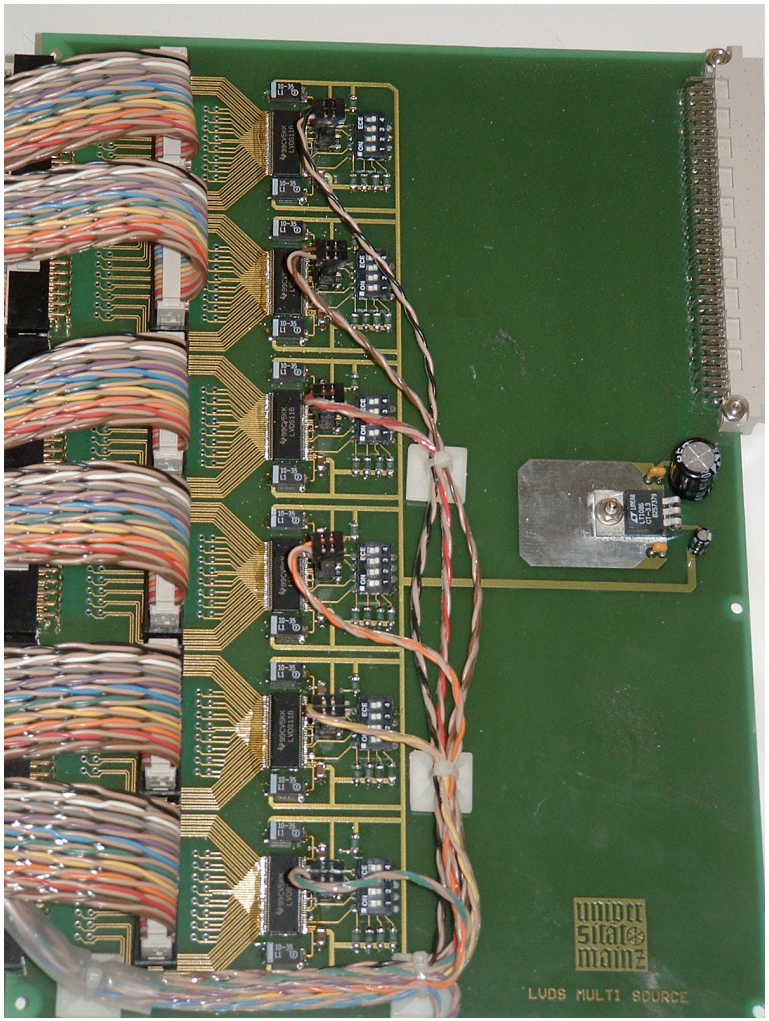
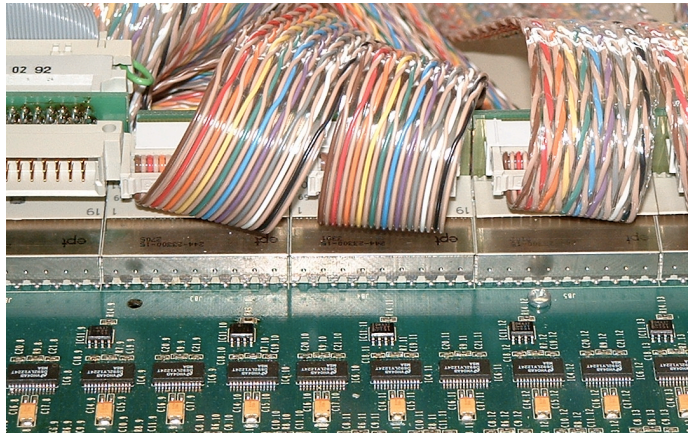
Link Replicator Module



- 96 channel LVDS fan-out
- source: 6 channel LVDS Serialiser from DSS
- 6 fan-out chips (TI LVDS116, 1:16)
- interface adapters to JEM0.0:
  - backplane link connectors
  - 2 m twist'n flat cables



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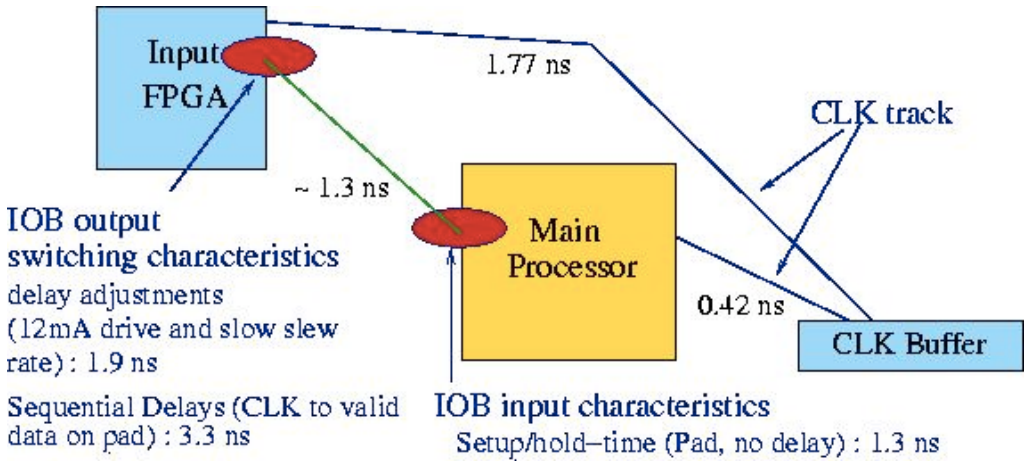
Link Test Results

- test patterns: 9 bit binary counter with odd parity from DSS data buffer memories
- 72 of 88 LVDS links sourced using Link Replicator Module (others not connectable yet)
- 64 of 72 channels: no link break (LOCK) or parity error in 6 hours of testing
- Reasons for link breaks:
  - interrupted serial tracks on PCB (JEM0.0)
  - signal quality of replicated channels is not ideal (jitter, signal levels) => links resynchronize
- power consumption of JEM0.0 : 7.1 Ampere

Test results of RTDP
- Interface between InputFPGAs and MainProcessor -

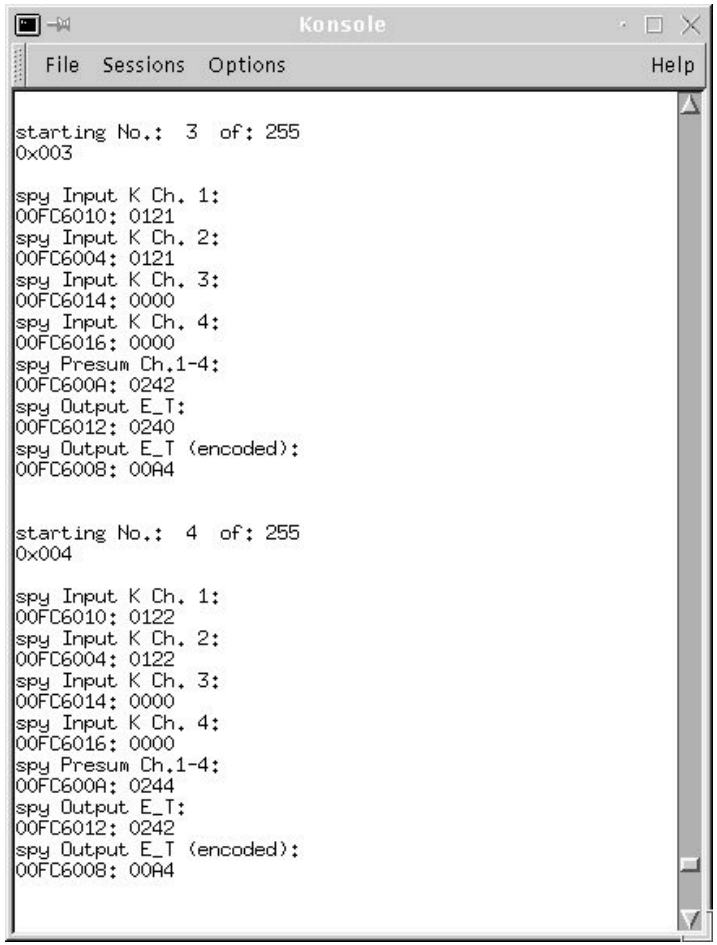
- problems with synchronisation of multiplexed data stream from InputFPGAs due to different track lengths
- IOB characteristics from Spartan II and Virtex E may yield to further delays (approximately ~ 5.2 ns)

- need more measurements to adjust clock phase of demultiplexing in MainProcessor



Test results of RTDP
- MainProcessor -

- data stream from all InputFPGAs available
- de-multiplexing needs timing adjustment
- E_T-tree implemented successfully
- quad-linear-encoding works
- spy memories for testing implemented
- needs:
  - E_X - and E_Y - trees tests
  - DAQ tests



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Firmware
- VME handling -

- VME access :
  - communication between ControlFPGA and each InputFPGA via asynchronous ringbus system
  - VME interface between ControlFPGA and other FPGAs (ROC and MainProcessor) operate synchronously

    => use IOB-FlipFlops
- incoming bidirectional VMEbus is separated into two unidirectional signals in toplevel code

  =>avoid bidirectional bus system on each chip!

```
---fan in/out of VMEbus (DATA)-----------

ts_en<= not s_write;

---split data path / tristate control of bidirectional port dat ----
p_IOFF:process(clk40)
begin
 if clk40'event and clk40='1' then
       s_data_in<=rdo_daq_d;
 -- inputs registered unconditionally
          if ts_en='1' then
-- registered and tristated if read
              rdo_daq_d<=s_data_out;
          else rdo_daq_d<=(others =>'Z');
 -- TFF replication done automatically
         end if;
 end if;
end process;
```

Firmware

- Readout Controller -

- VME access and registers implemented according to specs (JEM specification)
- activation of G-Links
- data mapping into bit pattern for slice readout (DAQ)
- still missing:
  - Functionality to determine bunch crossing number
  - Read out logic which supports existing DAQ logic of Input and MainProcessor FPGAs

Test vectors for JEM0.0 prototype

- based on adder tree for Fast Trigger Simulation (ATL1CT by Kambiz, Alan, Rolf et. al.)
- Options for tests:
  - test pattern like binary counter
  - „real – physics pattern“ like tt -> 4 jets from ATLFAST
- resorted to fit architecture (2 crates, Input FPGA labels, sum region)
- parity and encoding included
- To do:
  - Tool for loading JEM with vectors, readback from spy memories and comparing
  - Expand for Jet Algorithmen (Stockholm)
    (ROI available from ATL1CT)

```
Test Pattern: Counter 4 GeV steps, Input D-J
JEM Output to Merger:
             EX       EY       ET
plain:     2344     3547     2208
encoded: 36  3    55  3    34  3

word to CMM (25 bit): 14874596

Inp   Ch.          Input          Input      ET
FPGA                 em             had SumChk
K  1  1 h    0  1   512 e   0  1   512        0
K  1  2 h    0  1   512 e   0  1   512        0
K  1  3 h    0  1   512 e   0  1   512        0
K  1  4 h    0  1   512 e   0  1   512        0
J  2  1 h    0  1   512 e   0  1   512        0
J  2  2 h    4  0     4 e   4  0     4        8
J  2  3 h    8  0     8 e   8  0     8       24
J  2  4 h   12  1   524 e  12  1   524       48
H  3  1 h   16  0    16 e  16  0    16       80
H  3  2 h   20  1   532 e  20  1   532      120
H  3  3 h   24  1   536 e  24  1   536      168
H  3  4 h   28  0    28 e  28  0    28      224
G  4  1 h   32  0    32 e  32  0    32      288
G  4  2 h   36  1   548 e  36  1   548      360
G  4  3 h   40  1   552 e  40  1   552      440
G  4  4 h   44  0    44 e  44  0    44      528
F  5  1 h   48  1   560 e  48  1   560      624
F  5  2 h   52  0    52 e  52  0    52      728
F  5  3 h   56  0    56 e  56  0    56      840
F  5  4 h   60  1   572 e  60  1   572      960
E  6  1 h   64  0    64 e  64  0    64     1088
E  6  2 h   68  1   580 e  68  1   580     1224
E  6  3 h   72  1   584 e  72  1   584     1368
E  6  4 h   76  0    76 e  76  0    76     1520
D  7  1 h   80  1   592 e  80  1   592     1680
D  7  2 h   84  0    84 e  84  0    84     1848
D  7  3 h   88  0    88 e  88  0    88     2024
D  7  4 h   92  1   604 e  92  1   604     2208
C  8  1 h    0  1   512 e   0  1   512     2208
C  8  2 h    0  1   512 e   0  1   512     2208
C  8  3 h    0  1   512 e   0  1   512     2208
C  8  4 h    0  1   512 e   0  1   512     2208
```

Outlook

- Main task now:
  - put playback memory into operation
  - test of E_x – and E_y – tree
  - use test vectors for complete RTDP tests
- In parallel:
  - finalise firmware for readout controller
  - DAQ path tests