Processor Backplane Status

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- Backplane overview
- Recent developments
- Status of prototype crates
- Experience so far
- Plans and outlook

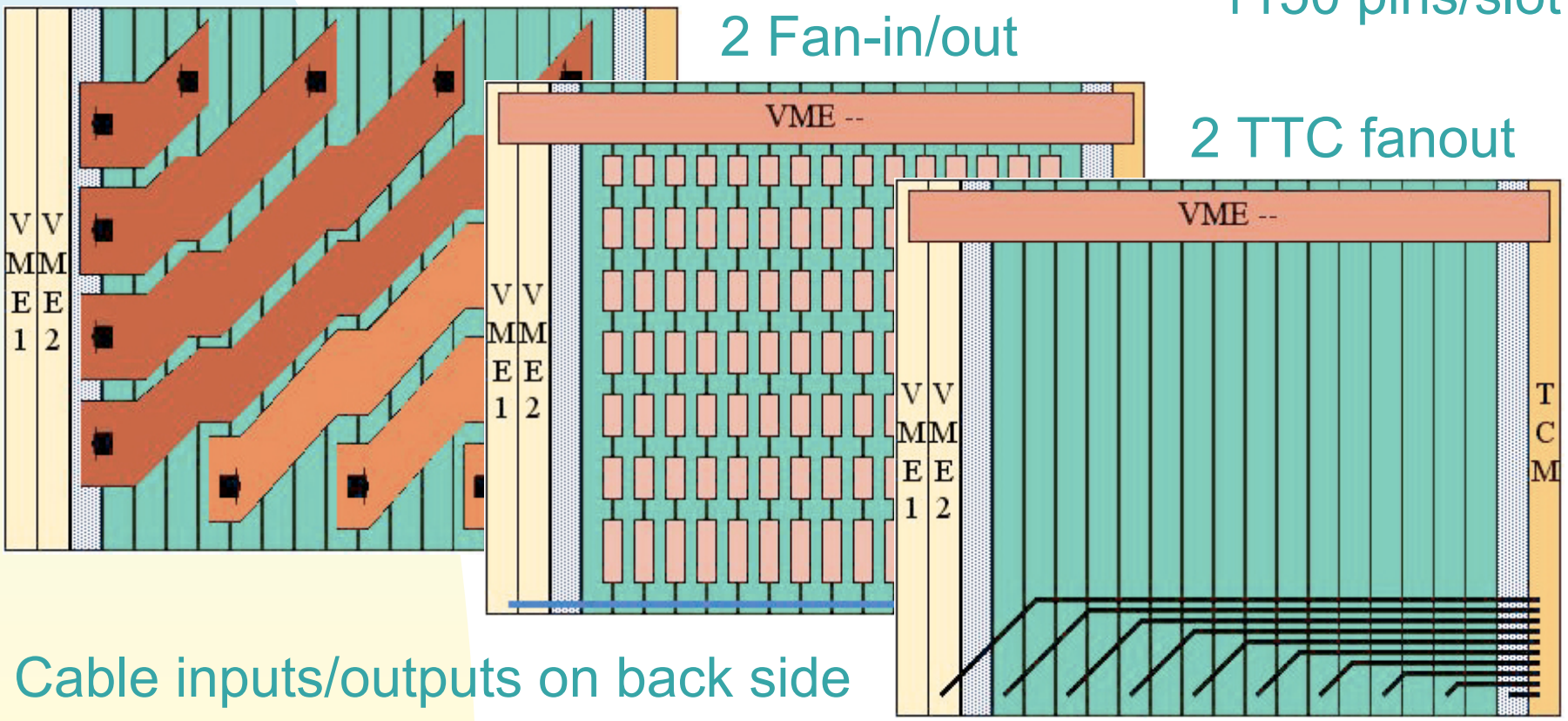
Processor Backplane

9U, 21 slots, 18 layers (8 signal)
Reduced VME, TTC, CAN
~1150 pins/slot

4 Merging Layers

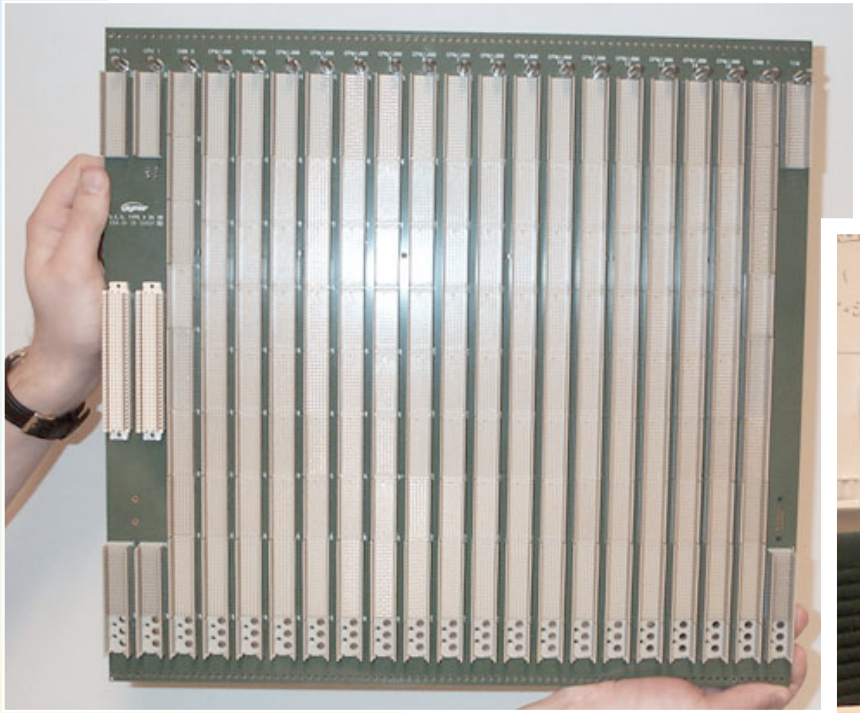
2 Fan-in/out

2 TTC fanout

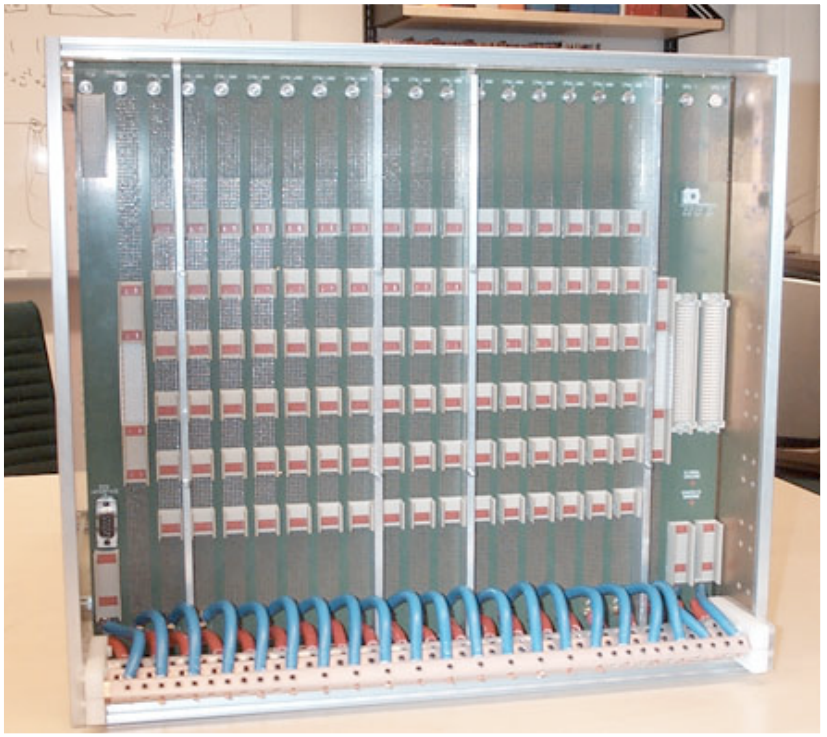


Cable inputs/outputs on back side

Processor Backplane



4 prototypes manufactured



Recent Developments

- Ground pins received after Heidelberg meeting
- Insertion tests at RAL, Birmingham show some bowing of modules
  - Future modules should have stiffening hardware
  - Improve situation by using longer guide rails
- Geographical addressing error found for CMMs
  - Subtle error found in schematics, understood.
  - Fix: extract one pin from slot 20

Status of processor crates

- Crate 1: Sent to RAL incomplete. Sent ground pin assemblies and long rails for upgrade. CMM GA0 modification?
- Crate 2: Sent to Birmingham incomplete. Ground pin assemblies and long rails sent later, crate upgraded. GA0 modification?
- Crate 3: Sent complete with GA0 modification
- Crate 4: To be sent incomplete to RAL, finished crate sent to Mainz for summer tests

Experience so far

- The backplane seems to work as planned
  - Modules fit in their proper places
  - VME--, CAN buses tested successfully
- Need to be careful during assembly
  - Chassis ground connected to crate by mounting screws (use washers if this is a problem)
  - Easy to damage rear shrouds, pins
- Rear bottom shrouds on TCM, CPU positions not very accessible (blocked by power cabling)

Plans and Outlook

- Parts of backplane still not tested:
  - Inter-module FIO, merging
  - TTC fanout
  - Geographical addressing
- Backplane testing, characterization in Stockholm
  - All four crates abroad over summer
  - Need one back in autumn for tests
- Should compile experiences for modifications to specification before final production