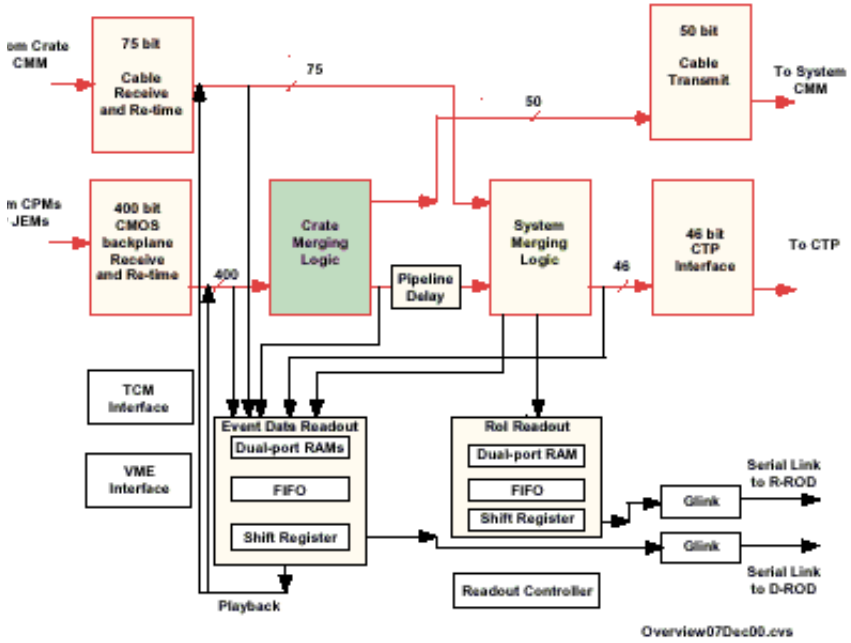
Common Merger Module, adapter modules and test cards: status & test plans

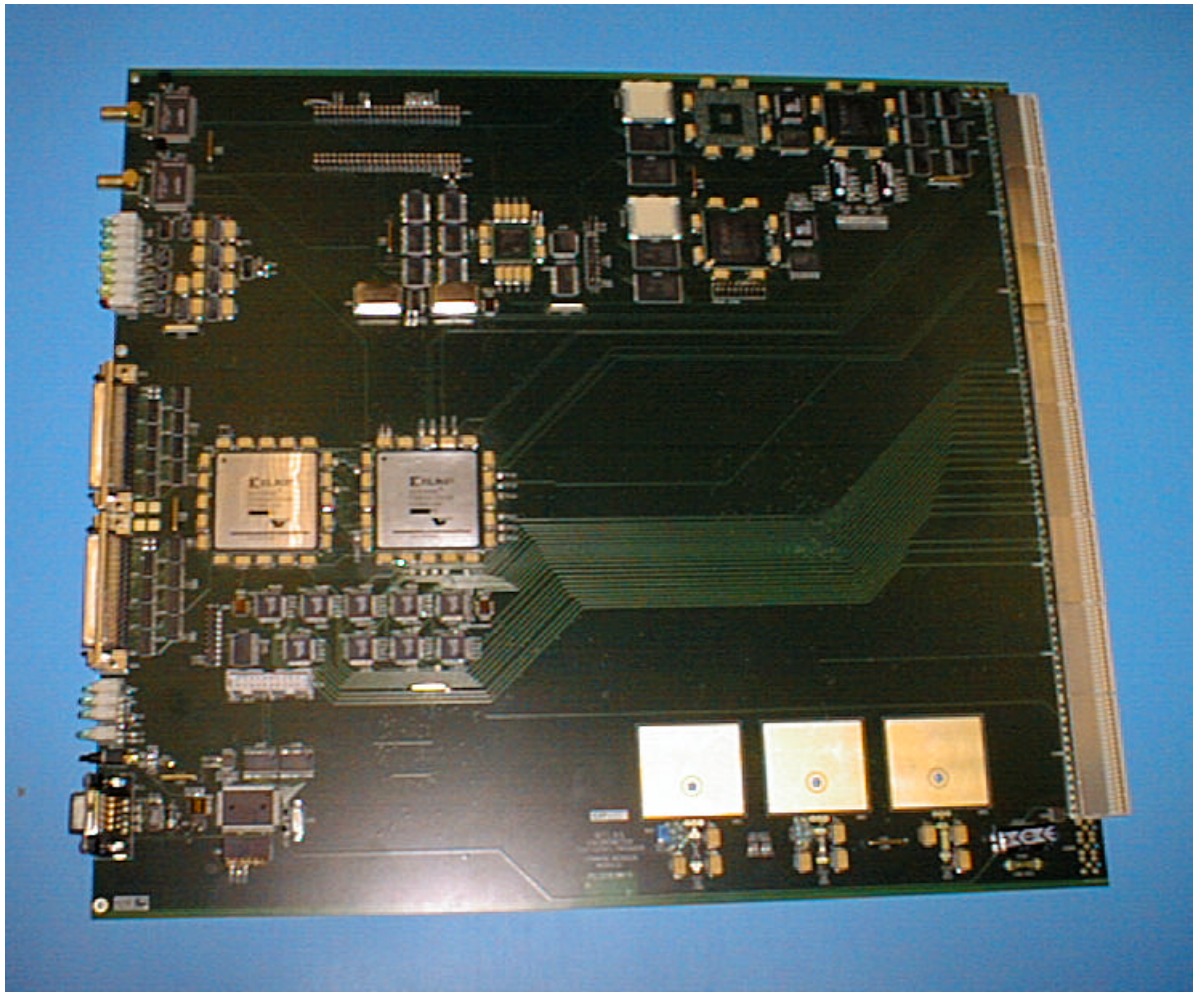
- CMM
  - –overview
  - –photograph
  - –current status
- RTM
  - –status
  - –photograph
- Test Plans

The Common Merger Module

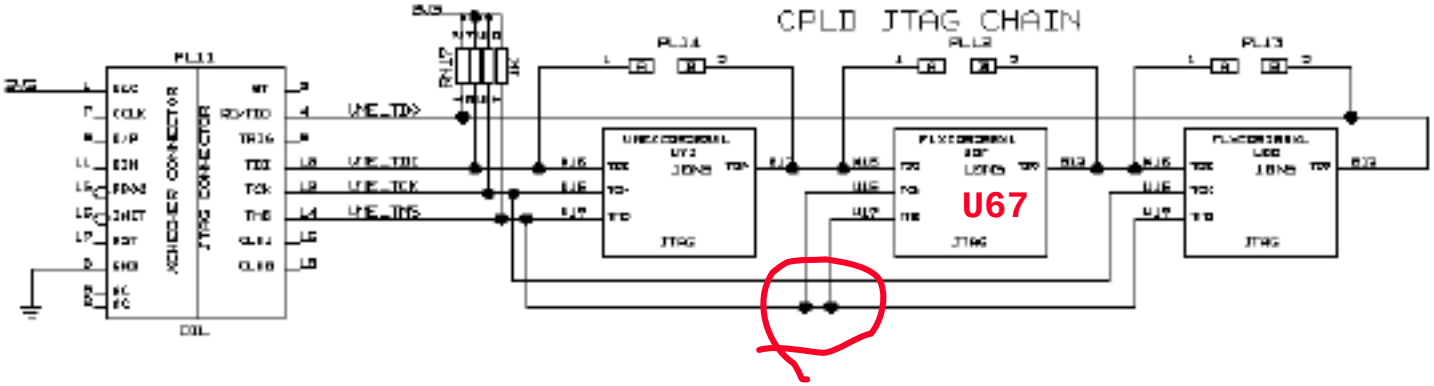
- CMM merges data from CPMs and JEMs:
  - e/? and ? hit counts
  - jet counts
  - jet energy sums
- Within each system 2 CMM types:
  - Crate CMMs: crate level merging
  - System CMMs: crate + system level merging
- Algorithms implemented using field-programmable devices:
  - Crate FPGA (XCV1000E-FG860)
  - System FPGA (XCV1000E-FG860)
- Flash memories contain all configurations
- CMM configured to required type according to geographical address & crate no.



CMM: The Photograph



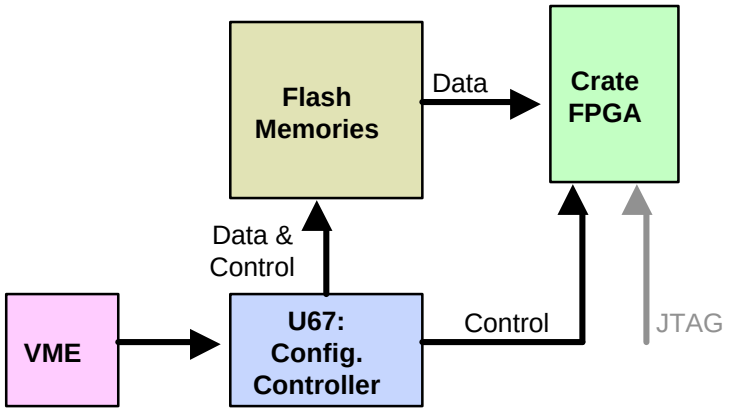
CMM: The JTAG problem



- Problem found by software whilst preparing for JTAG tests:
- U67 JTAG input TCK (clock) tied to TMS (control) by mistake.
  - ? Cannot drive or load U67 by JTAG.
  - ? U67 will output junk to JTAG chain.

- JTAG required to configure these CPLDs.
- Problem discovered after manufacture, buried beneath BGA.
- One board assembled with U67 absent
  - allows rest of CPLD JTAG to be used.

CMM: The JTAG problem, continued



- U67 is Configuration Controller for Crate FPGA.
  - ? current module cannot be made to configure Crate FPGA automatically at power up.
  - ? Another design iteration will be necessary.

- Meanwhile, with current module:
  - FPGAs can be configured via FPGA JTAG chain.
  - Cannot test Configuration Controller for Crate FPGA.
  - Can test Configuration Controller for System FPGA, and *everything else*.
- Test as much of current module as possible before proceeding to second design iteration.

- What can we learn from this?
  - Prepare for JTAG tests before the design goes out to manufacture.

CMM: Progress & Status

- Connectivity
  - JTAG found one missing connection: Crate FPGA - System FPGA
    - can re-route signal via spare track
  - we found one further missing connection: System FPGA - test connector
  - need to investigate causes of these failures

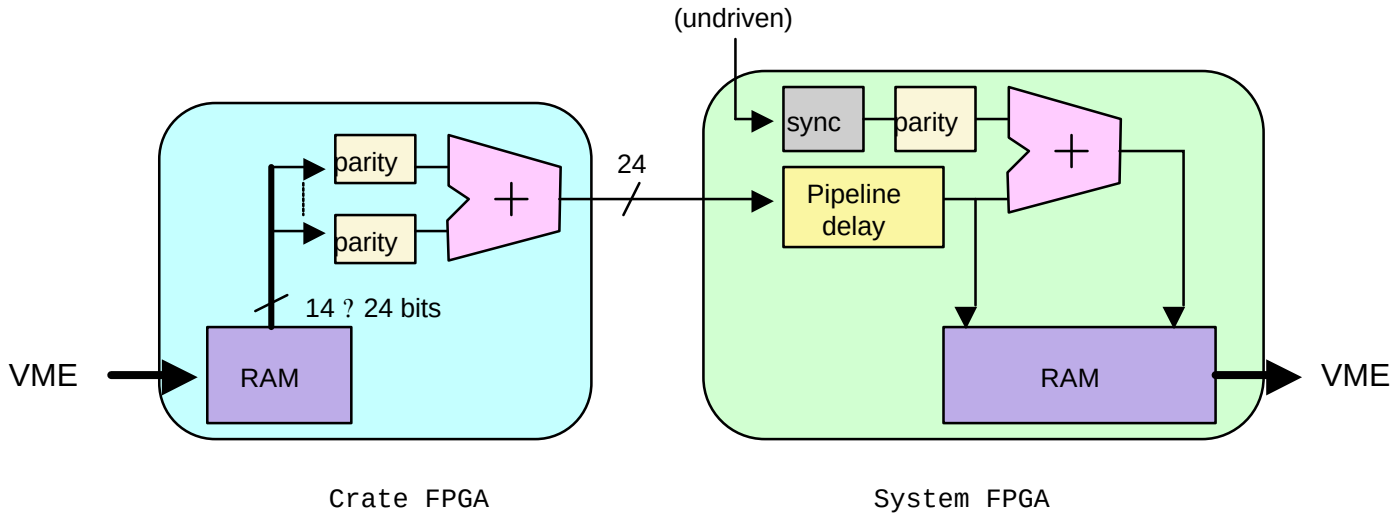
- JTAG programming of FPGAs works.

- VME interface OK so far…
  - Address decoding works
  - Can't test all control and status bits yet, but those tested are OK
  - Read & write access to FPGA RAM space OK.

- Corrected number of minor bugs in firmware and hardware
  - no show-stoppers yet.

- Operated the CP System CMM in playback mode.

CMM: Playback Mode

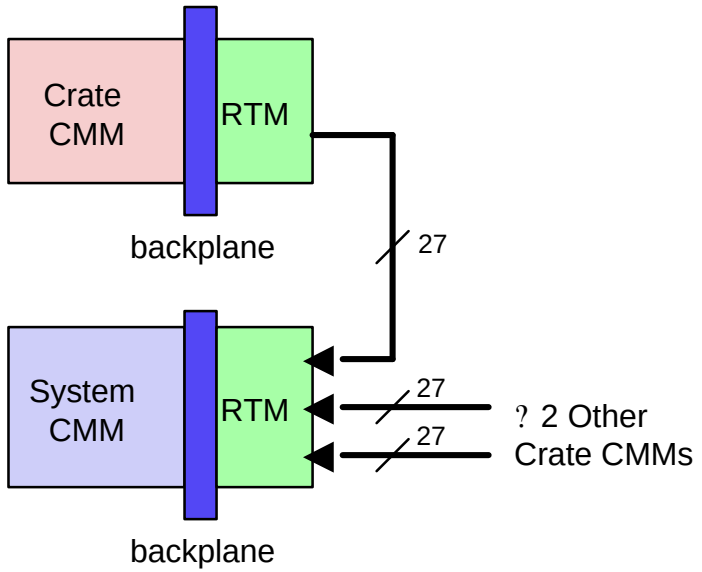


- Data has been transferred successfully from Crate FPGA to system FPGA
- Demonstrates operation of
  - VME-RAM interface
  - parity-checking logic
  - result merging logic
  - initial stages of readout logic
- Tests not exhaustive.

CMM Rear Transition Module (RTM)

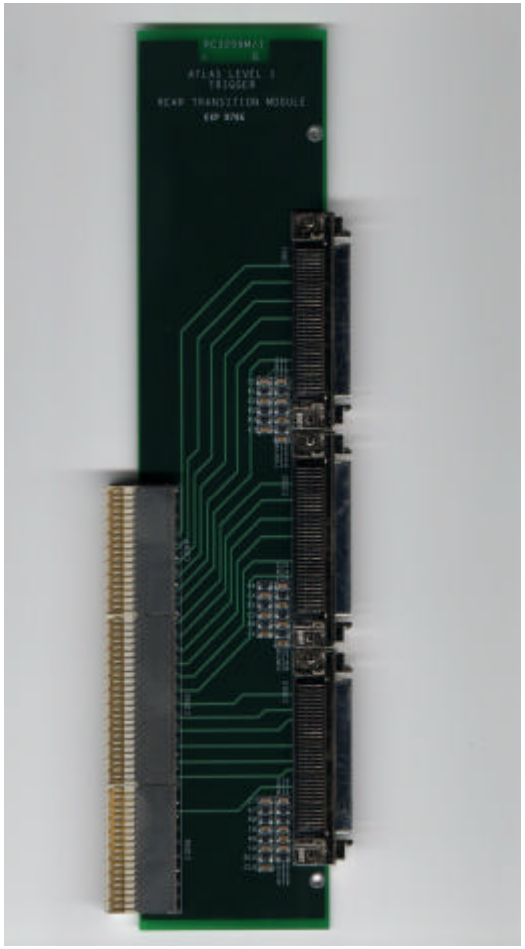
- **Signals transferred from Crate- to System level CMMs via SCSI-3 cables.**
- **Each cable carries 27 differential pairs.**
- **Signals pass to/from CMM, through backplane, as differential LVDS pairs.**

- **RTM :**
  - **Maps signals from backplane pins to 3 SCSI-3 connectors.**
  - **Passive module.**
  - **Will be supported on back of crate by two aluminium bars with guide slots carved into them.**



RTM: Status

- One module arrived back from assembly 3rd July 2002 (i.e., about half an hour ago).
- Not yet tested.



CMM Test plans

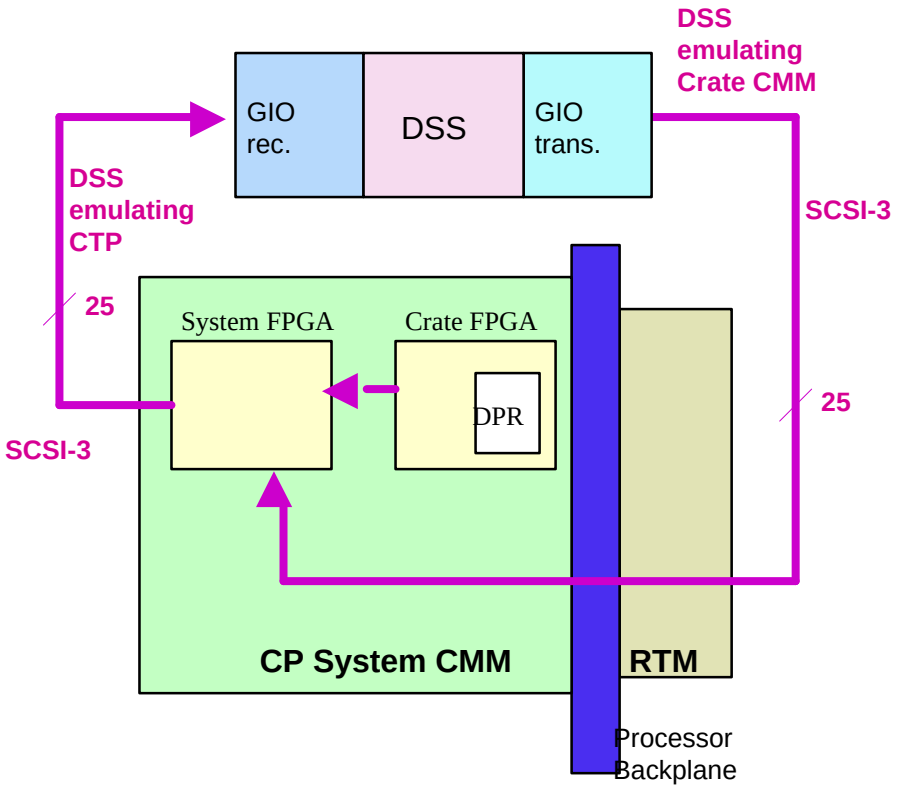
CMM testing: Next steps:

- **Get configuration controller working for**
  - **Flash ? System FPGA.**
  - **VME ? Flash.**

- **Test real-time data paths:**
  - **currently assembling test system in Electronics lab at RAL to do this.**
  - **Require:**
    - **CMM**
    - **RTM**
    - **ATLAS trigger crate, TCM, VMM**
    - **DSS**
    - **GIO**
    - **CPM slot adapter.**

CMM System FPGA tests

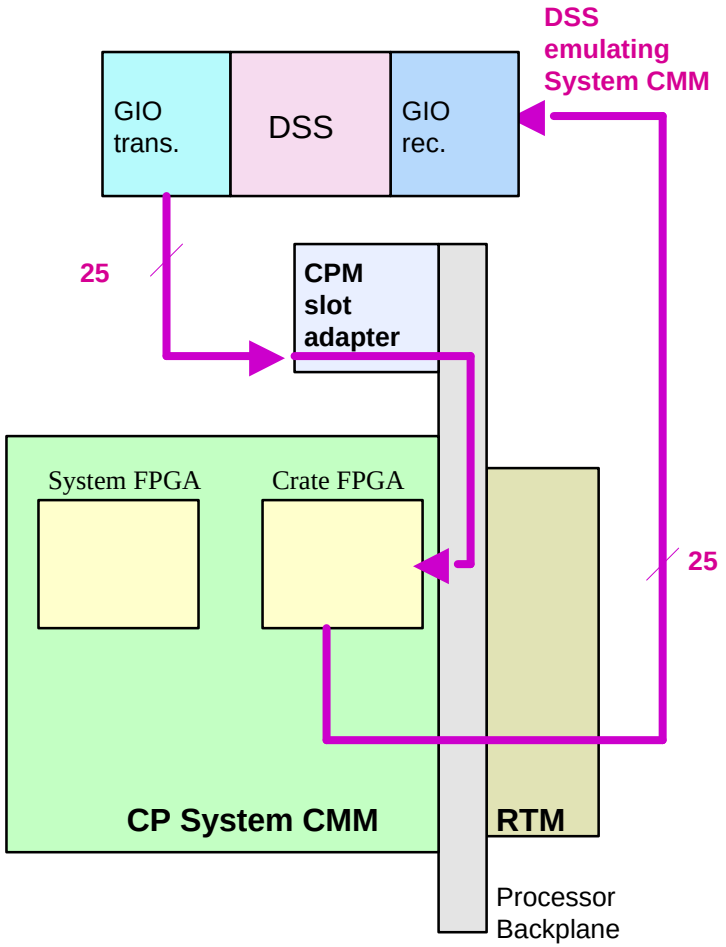
- This will test
  - RTM
  - CMM LVDS inputs
  - integrity of 40 MHz signals across board
  - synchronisation logic
  - parity-checking logic
  - merging logic
  - parity-calculating logic
  - Connection to CTP.



CMM Crate FPGA tests

- This will demonstrate:
  - synchronisation logic
  - parity checking
  - merging logic
  - LVDS outputs.
- Use CPM slot adapter made by Richard Staley.
- Wont fully populate inputs; just demonstrate vertical slice through module.

- After this,
  - Crate + System FPGA tests…
  - Readout logic tests….



Summary

CMM :

- the following have been tested and found to work:
  - loading of FPGAs via JTAG
  - DLLs in FPGAs
  - VME interface
  - Playback mode transfer of data Crate ? System FPGA
- However, so far tests have not been exhaustive.
- Next steps:
  - Get configuration controller working for
    - Flash ? System FPGA.
    - VME ? Flash.
  - Test real-time data paths.

RTM:

- One module just arrived back from assembly.

Test rack:

- Currently being built