CPM Tests Status

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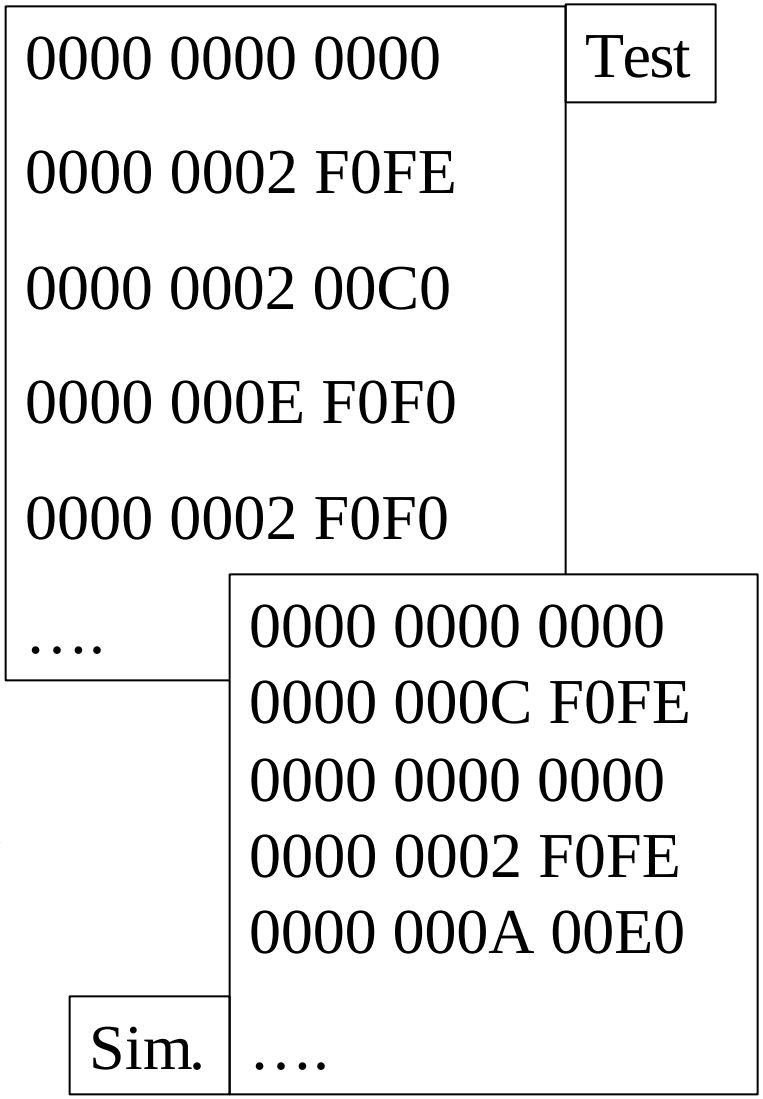
CPM – Firmware Status :Srl and CP

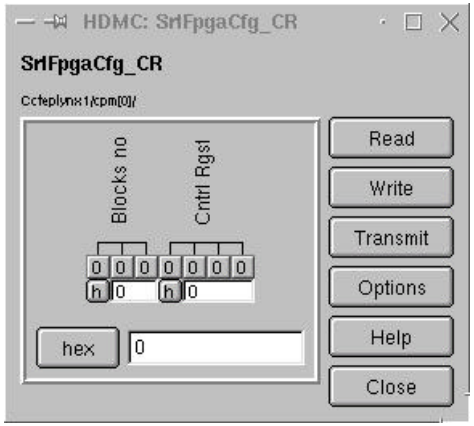
- 20 Serialisers loaded: DPR problems corrected: no corrupted data appearing randomly anymore
- 1 CP chip loaded in ScanPath Mode:
  - All channels calibrated correctly except 4 of them
  - During early tests, try to sold a wire on board to read data. It has partly damaged some resistors.
  - Resistors changed but still 2 channels does not answered:
    - On the e.m. side, srl V to cp chip 1: the calibration is not working for this channel too, double checked with a new BS?
    - On the Had side…but the calibration process works for this channel! Always read the same value 0x8 whatever you sent to it.

CPM – Firmware Status :CP

- CP real mode:
  - Weird: calibration works for all the channels, even the faulty one see in ScanPath mode
  - DPR works
  - First Algorithm investigation:
    - Load test vectors and threshold used for the CP simulation but setting 0 to all non available input
    - Data were available in the DPR
    - Run CP model with same data input
    - Data available in DPR not exactly the same but very similar
    - CP algorithm looks running OK!



CPM – Firmware Status :VME Controller



- In order to download other F/W from the same FlashRam, VME controller modified with a block number to select the device
- (Fatal?) Warning: all the F/W file to be downloaded belong to the same device…wrong file could be recognised and downloaded…and the FPGA damaged due to wrong IOs layout.
- DAQ ROC successfully downloaded

CPM – Firmware Status :DAQ ROC

- Some bugs discovered in the F/W not seen in simulation:
  - Access to DPR
  - Control Register ignoring an Enable Data In signal
- To test data flow,it required a modification to generated a Lvl1A signal, either in the TTC controller or in the Daq Roc f/w itself

CPM testing: more software needed

- Early tests required a lot of time by downloading independently each DPR and set of threshold, Control Register,…so far done with Hdmc via Gui
- CPM services are available..just need time to write all the services
- Automatic testing could then be performed

CPM: Future Tests to be performed

- Download other set of CP and Serialiser chips to avoid faulty links
- Complete test Daq Roc + Glinks path
- Download RoI Roc F/W
- More CPM Services to be written
- Bring external LVDS signals to test receivers:
  - Need Dss+ Io cards and theirs sofware
- TTCdec interaction via I2C bus