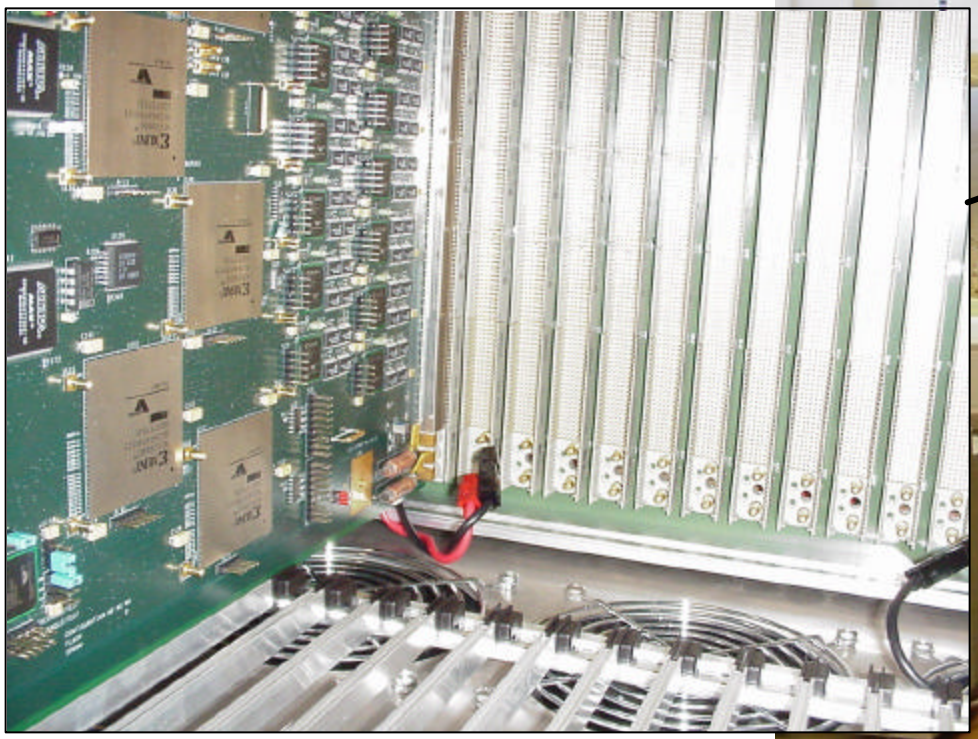
CPM Testing –
CP chip simulation

CPM Testing Setup

- The setup is :
  - One 6U crate with CPU Cct + TTCvi + TTCvx + Bit3
  - One 9U L1 crate with VMM with Bit3 + CPM + TCM
  - One PC with Linux 6.2 + HDMC
- Bit3 system enable us switching off L1 crate crate without rebooting.

System Test



S/W

- Bit3 code written to initialize mapping 6U and 9U crate (“Bit3”)…could be implemented as a new part for HDMC.
- New part created: FpgaFlashRam to download Fpga code inside Flash Ram of the CPM…not working yet so far

Tests results so far…

- TCM:
  - Id read
  - F/W version read
  - Data Display does not work if not TCM?
- CPM:
  - Recover Motherboad ID, F/W version (Richard's) after bypassing GeoAddr
  - Write to Control Register
  - Write to FlashRam F/W under treatment

Next steps

- Load one Srl device
- Test VME access Srl chip
- Test PlayBack Memory + Calibration pattern (Spare pins?)
- Load others Srls + CP chips
- Test Calibration Cp chip
- Testing connectivity between SRL and CP Chip at high speed
- Testing partial shared signals with loop-back board
- PS: to have a SRL chip VHDL model could help debugging?

CP chips model

- Received VHDL CP chip code at gate level with its timing file (time_sim.vhd and time_sim.edf)
- Previous latency given was read without taken into account the choice of device
- Problem with VME access, might be OK
- Can’t simulate more than 300µs due memory problem (too many warnings)
- Algorithm latency will be more difficult to measure