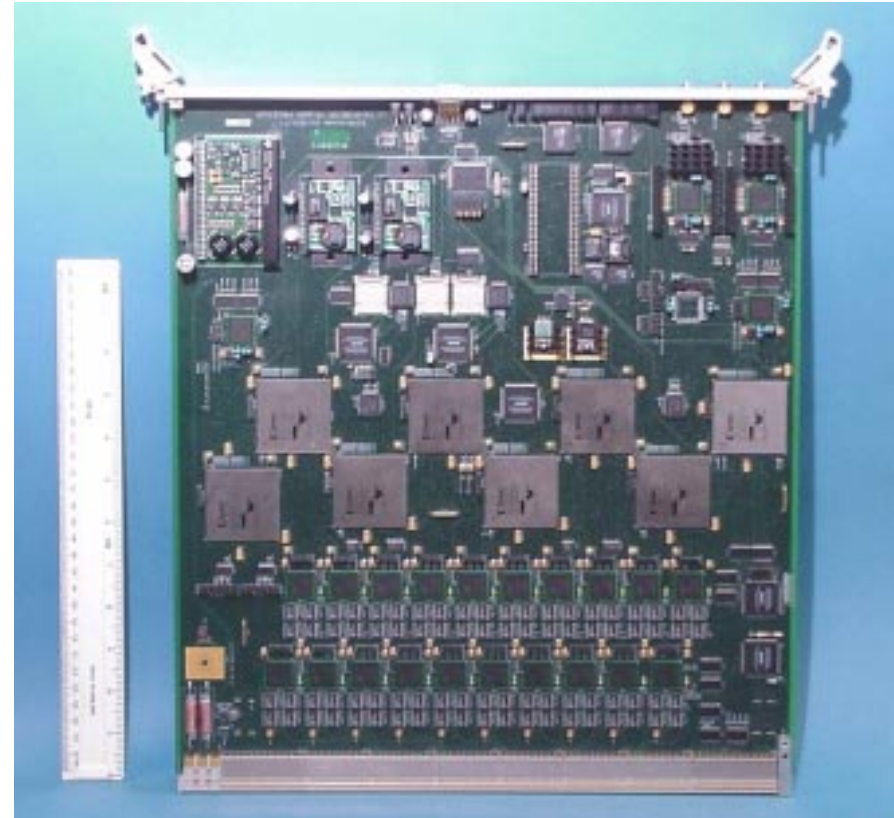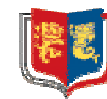# CPM Prototype Hardware

- Documentation

- The story so far …

- FLASH memory

- Next

- Test Cards

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Documentation

User Guide (Hardware)

http://www.ep.ph.bham.ac.uk/user/staley/CPM_USER.pdf

PCB Modifications

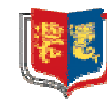http://www.ep.ph.bham.ac.uk/user/staley/CPM_MODS.pdf

Programming Memory Map

http://www.ep.ph.bham.ac.uk/user/staley/CPM_MM.pdf

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ATLAS Level 1 Calorimeter Trigger (UK) Meeting   RAL   15/5/2002

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The story so far …
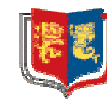
JTAG / BS testing was a **success**!

All detected assembly faults have been corrected.

Test coverage was not 100%. Connections not tested:

- Backplane Connector
- LVDS de-serialisers
- G-Link Tx

For production the JTAG / BS test set-up must be expanded to check the connector path using an external BS device.

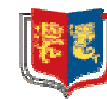**R. Staley**

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- **All CPLDs programmed OK from PC.**
(VME interface , Flash controllers and LED display)

- **TTCRx Interface FPGA configures from Serial EEPROM.**

- **CAN controller sometimes runs HOT.**
Depends upon power-supply used.
CAN Rx LED flashing. What does it mean?
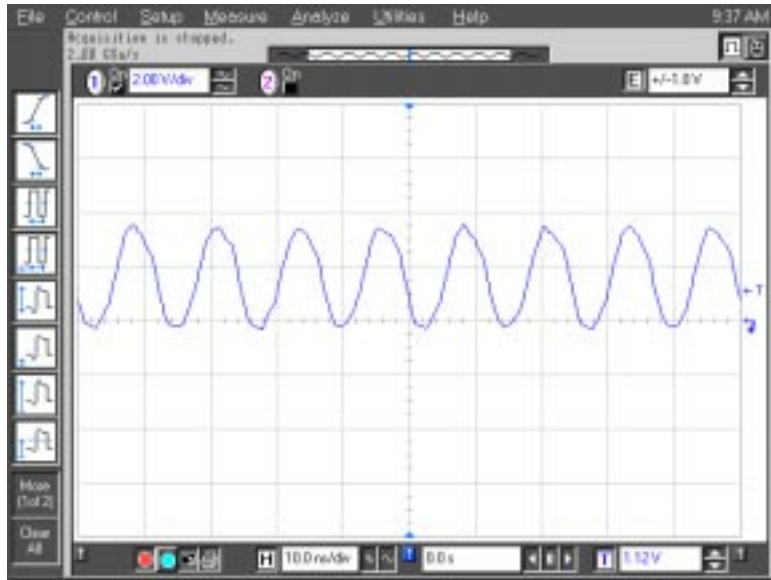

- **Clock distribution (using dummy TTCDEC)**

Wire added and a terminating resistor moved.

Three PLL devices need replacing…
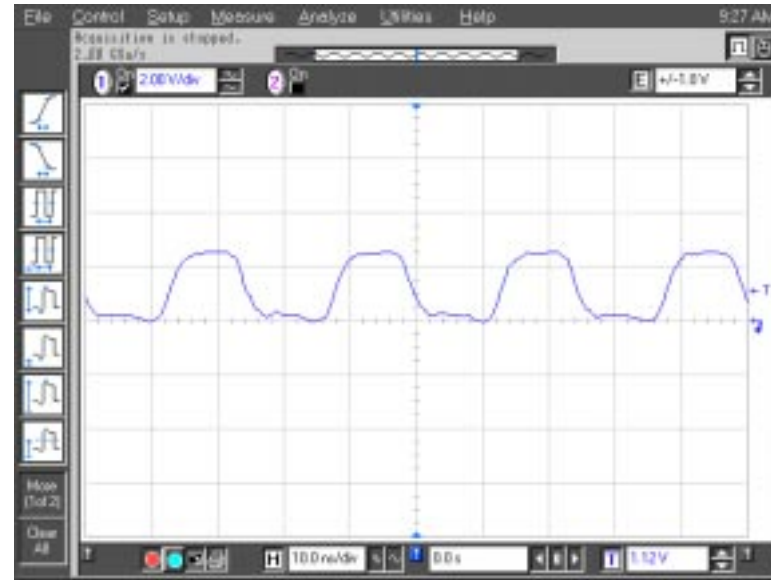

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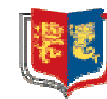The version fitted , x2 certain clocks to 80MHz.
CY2308SC-4 should have been CY2308SC-1.

Clock input to G-Link - WRONG   Clock into CP FPGA - CORRECT

Correct parts can be fitted at Birmingham.

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- **VME interface now working.**

'Problem' ,due to unassigned pin of CPLD, now fixed.

Problem with Geographical Addressing, now disabled.
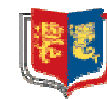Module or Backplane at fault? Untested by JTAG
Will investigate.

However we can:

    Access all CPLDs

    Read module ID and revision registers

    R/W and Erase FLASH memory via Configuration Controllers.

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FLASH memory

To program a FLASH memory , each word to be written has to be preceded by a 'command' sequence:

Command	Length	Bus Write Operations										
		1st		2nd		3rd		4th		5th		6th	
		Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Program	4	AAA	AA	555	55	AAA	A0	PA	PD				
Chip Erase	6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10

Note: X Don't Care, PA Program Address, PD Program Data.
All values in the table are in hexadecimal.

All this is handled by the FPGA Configuration Controller (FCC).

Software simply writes the desired contents sequentially into a FIFO.

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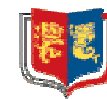
Next

Replace Clock Distribution PLL with x1 version.

Investigate Geographical Addressing problem

Check-out CAN uC overheating.

Obtain TTCDEC card and test TTCRx Interface

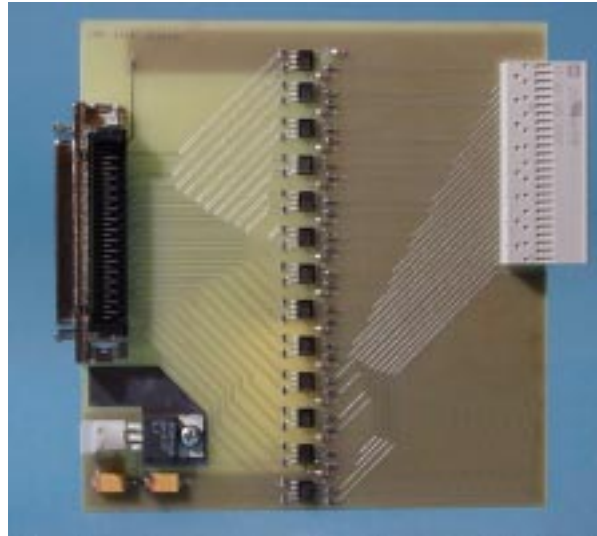Configure a Serialiser FPGA, then configure a CP FPGA.
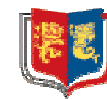
Configure all Devices.

…

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Test Cards - Status

- DSS-CPM slot adaptor - 1 prototype made.
  Order N more …

- DSS-CMM slot adaptor - 1 prototype made
  Order N more …

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CPM FIO loop-back

- PCB with single backplane connector that could be configured (linked) to loopback FIO signals from an adjacent slot containing the CPM under test.
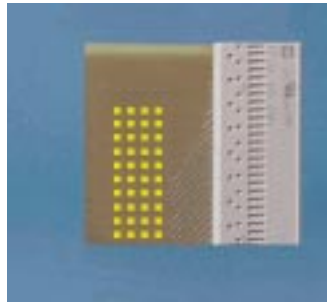
Problem. Pitch of FIO groups do not match that of the connector. Some links must cross connector boundaries.

http://www.ep.ph.bham.ac.uk/user/staley/

Backplane_FIO_colour.pdf

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Prototype/Production JTAG / BS Tests

- Must check the connectivity from the CPM backplane connector to the Serialisers and CP FPGAs. Also VME.

An external card (with an un-programmed FPGA) would allow this to be done using the RAL JTAG tester .
Could be mounted as a 'backplane' in a spare crate, to provide power and cooling. …

…comments please …

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