CPM Prototype

Hardware Status

- Documentation
- JTAG / BS Testing
- Next
- FLASH memory
- FPGA configuration

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Documentation

Draft user guide and updated memory map at:

http://www.ep.ph.bham.ac.uk/user/staley/CPM_USER.pdf

http://www.ep.ph.bham.ac.uk/user/staley/CPM_MM.pdf

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JTAG / BS testing

Module powers-up OK with on-board power-converters supplying correct voltages.

JTAG / BS testing was a **success**!

All detected assembly faults have been corrected.

A Quad Flat-pack had a number of pins unsoldered.
No faults were detected with connections to the BGA packages.

Test coverage was not 100% but pretty close.
What connectivity hasn't been tested:

- Connector pins
- LVDS de-serialisers
- G-Link Tx

(In production the BS test set-up should be expanded to check the connector path using an external BS device.)

Did observe the CAN controller running HOT. Not usual for a CMOS device. Device had not been programmed.

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NEXT

The CPM will come to Birmingham, for programming the ALTERA CPLDs.

The crate is not needed at this stage.

Once crate #2 is at B'ham we will continue with testing:

- Clock distribution
- VME access
- Configuration access.
- …

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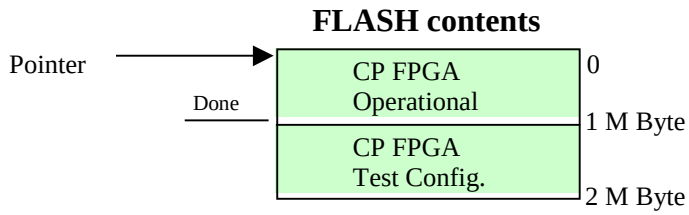
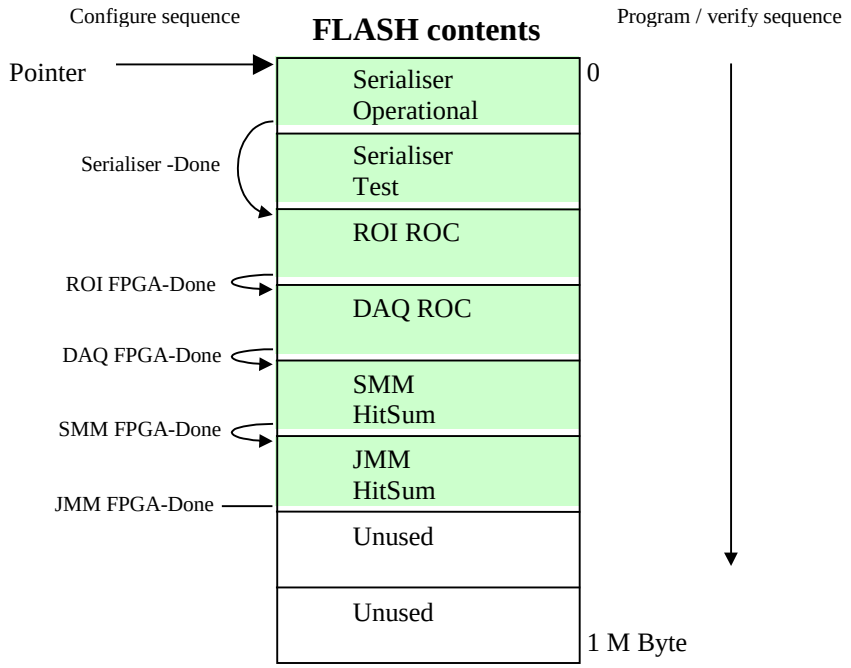
FLASH memory

Two different 'blocks' of FLASH memory (non-volatile) hold the configuration data for the XILINX FPGAs.

CP 'block' use two 1Mbyte devices:



Serialiser, ROC and HIT 'block' use one 1Mbyte device:



Need to combine the individual configuration images.

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FPGA Configuration

The FPGA configuration controller (FCC) design has been simulated (but not 100%) with FPGA configuration and FLASH access shown to perform as expected (by RJS) on power-up.

Once the configuration controller CPLDs are programmed, they will try to load all the FPGAs at the next power-up. Is this wise?

- FLASH configuration memories must be pre-programmed and fitted…
- FPGA Configuration should only be started from a VME command (for now?)…
- Effects of loading corrupted data into an FPGA.
  If CRC check fails then configuration is halted, right?

For the initial tests, the FCC design will be changed so that it attempts to configure only 1 FPGA, with all others permanently disabled.

….Comments please ….

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