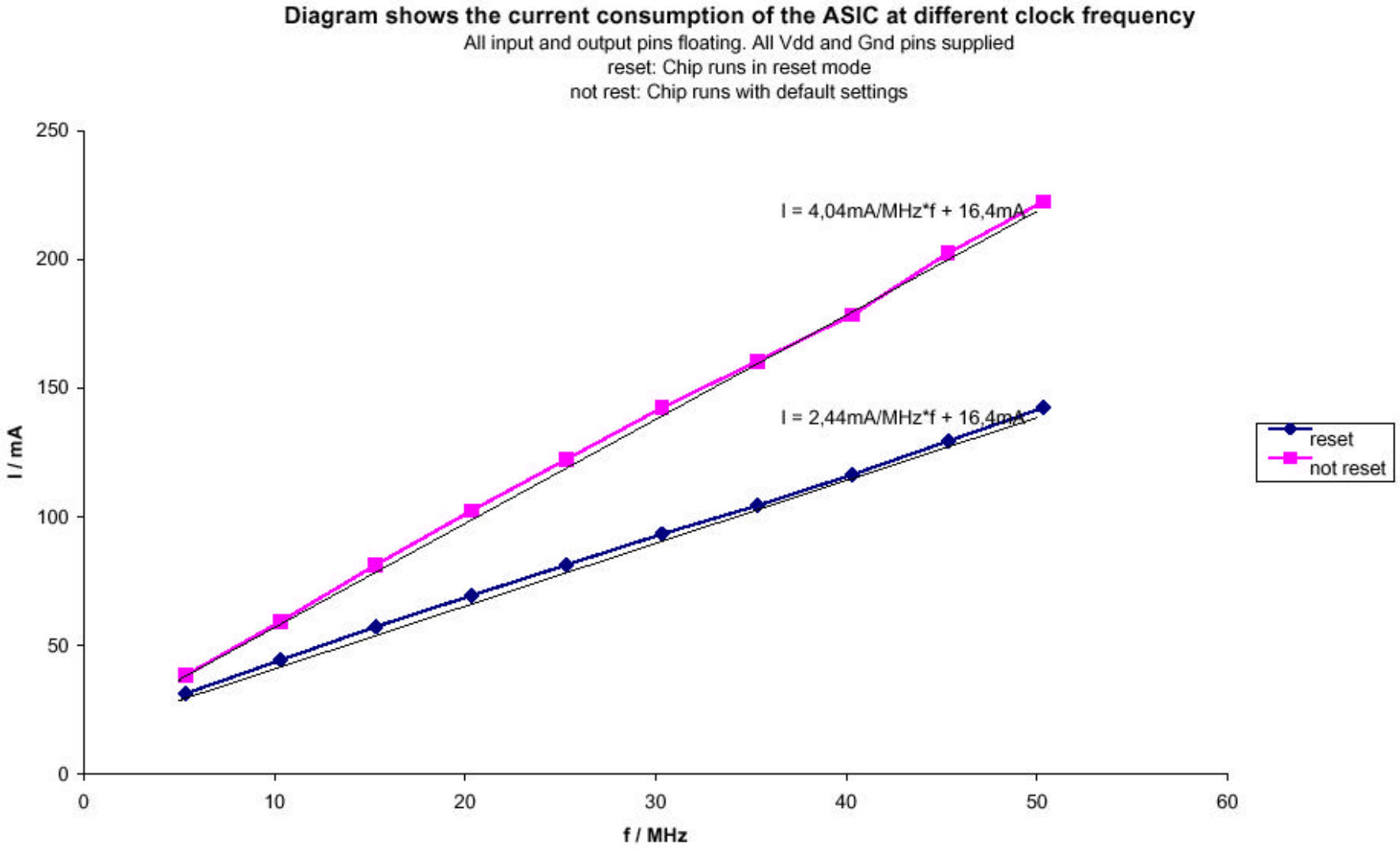
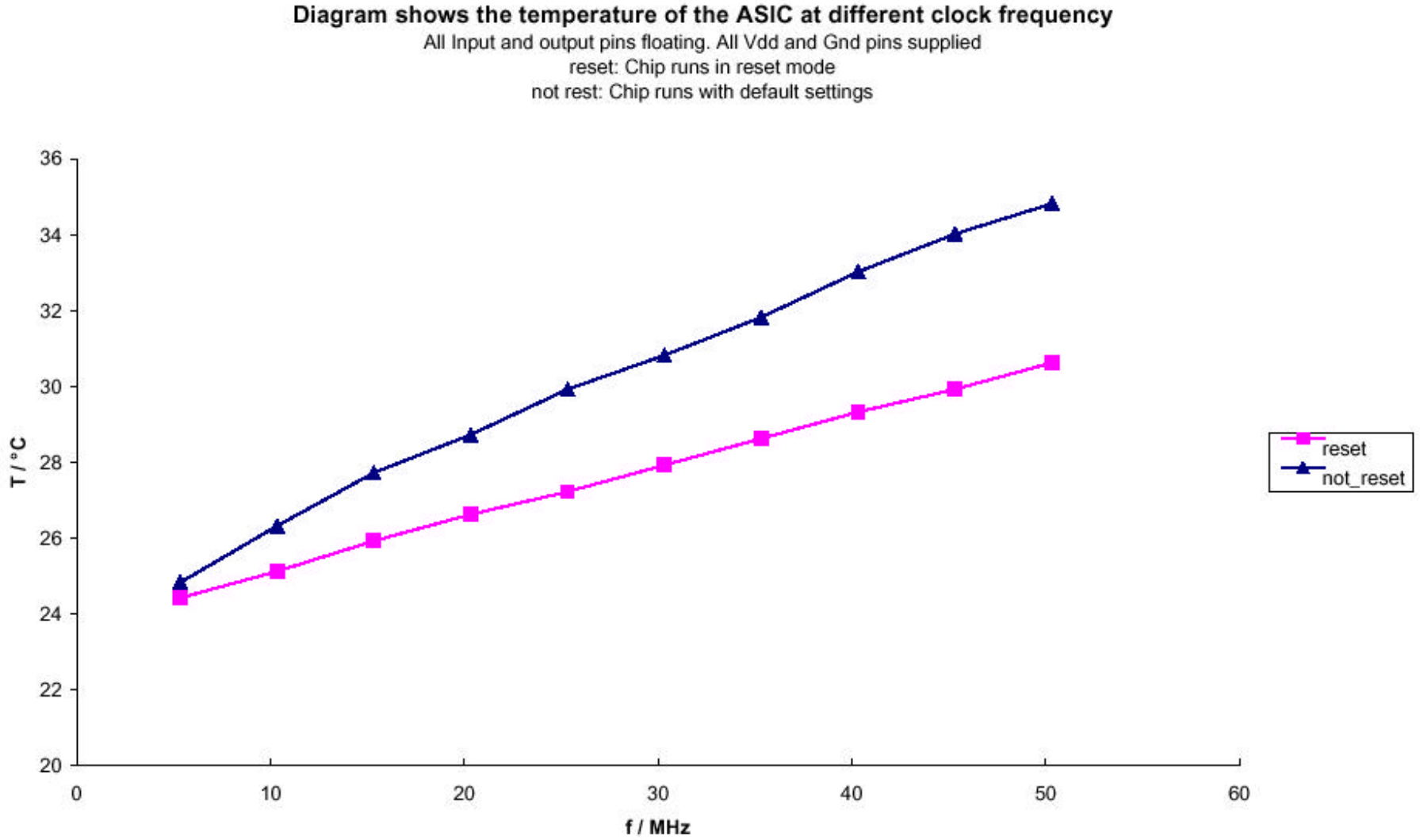
Heidelberg Status

- PPr ASIC fabrication complete
  - 160 chips diced, 1 PLCC-packaged, 2 undiced wafers
  - Supply current *vs* clock frequency tests look sensible *(linear)* – *e.g.* 175 mA at 40 MHz
  - Currents only ~25% of estimated values – open-circuit inputs → far fewer F/Fs toggling?
  - Needle probe cards will pre-select further dies for MCM bonding *(no more packaging)*
- PPR MCMs – 1-2 devices will be assembled at Heidelberg before end-April
  - All components (FADC, PHOS4 dies, substrates, lids, etc) available in "Slice Test" nos
- MCM-adapter test board routing will be completed by end-April
- ReM FPGA design – synthesis → XCV1000E CLB utilisation ~200%!
- No further news on PPM or PPr ROD

PPrASIC Clocking Tests 1



PPrASIC Clocking Tests 2



Mainz Status

- Computer and software upgrades have delayed the test programme
- JEM-0 #2 – JTAG tests are now working
- VME protocol firmware under control – simulation complete by end-April
- Test-Bench for real-time data-path now being written
- Full JEM tests require HDMC – currently being prepared
- Completion of true "Module-0" JEM design will probably be delayed until existing JEMs are fully-tested
- There may be only 2 JEMs *(#1 and #2)* available initially for the Slice Tests

Stockholm Status

- Assembly of all four crate/processor-backplanes (CPB) almost complete
  - Missing ground supply pins being shipped from USA directly to Stockholm
  - 1st CPB at RAL – already used for initial CMM, CPM, TCM and VMM testing
  - 2nd CPB will be shipped to UK ~18th April – for use with CPM at Birmingham
- Problems noted with CPB so far:
  - Module runners too short (280 mm) – 320 mm replacement runners will be ordered
  - All UK pcb-edges milled down from 2.0 mm to <1.6 mm for "expected" 1.6 mm runners!
  - BUT – JEM0 edge thickness remains at 2.0 mm and CPB runners are also 2.0 mm
  - Therefore we will standardise on 2.0 mm and add 0.4 mm shims to UK board edges
- Connector pin lengths not staggered → insertion forces ~20% higher
  - Module warp *(from assembly)* → bowing on insertion → 2-d bracing hardware needed
- Jet algorithm firmware simulations are continuing