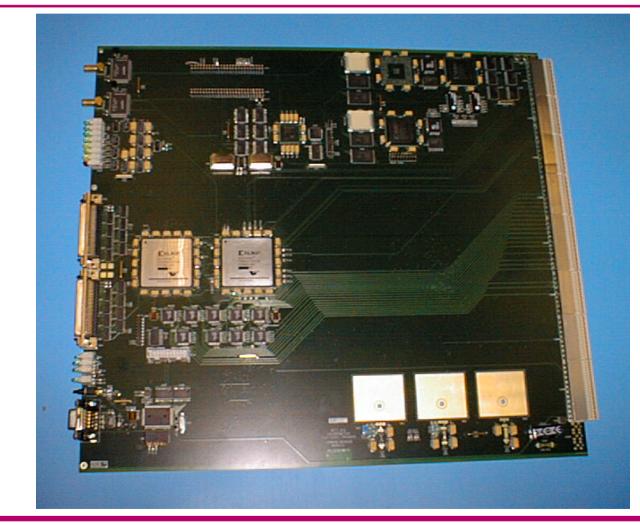
# The Common Merger Module: Status Report

- Photograph
- Hiccup
- Current Status



# **CMM:** The Photograph

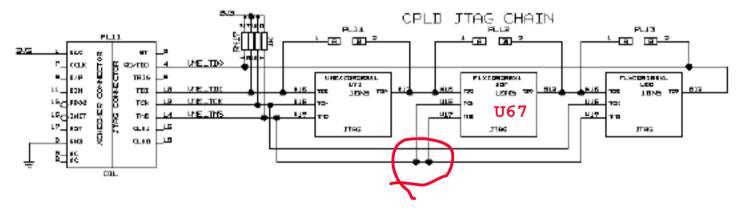




**CLRC** Instrumentation Department

Ian Brawn, 16<sup>th</sup> April 2002

# CMM: The JTAG problem

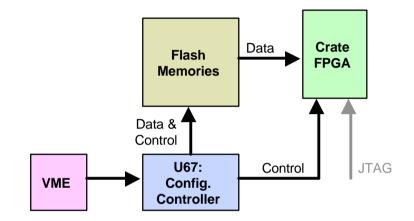


- Error found by Richard Matson whilst preparing for JTAG tests.
- U67 JTAG input TCK (clock) tied to TMS (control) by mistake.
  - ? Cannot drive or load U67 by JTAG.
  - ? U67 will output junk to JTAG chain.

- Two boards being assembled at the time....
- Problem buried beneath BGA....
- Cancelled assembly of one board.
- Other board assembled without U67, so that rest of CPLD JTAG chain to be used.



### CMM: The JTAG problem, continued



- U67 is Configuration Controller for Crate FPGA.
- ? current module cannot be made to configure Crate FPGA automatically at power up.
- ? Another design iteration will be necessary.

- Meanwhile, with current module:
  - FPGAs can be configured via FPGA JTAG chain.
  - Cannot test Configuration Controller for Crate FPGA.
  - Can test Configuration
    Controller for System FPGA, and everything else.
- Test as much of current module as possible before proceeding to second design iteration.

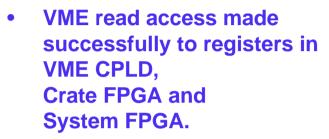
#### What can we learn from this?

• Give schematics to Richard Matson before the design goes out to manufacture.



## **CMM: Current Status**

- Error in Schematics uncovered during preparation for JTAG tests.
- One CMM received from manufacturers
- JTAG tests show one signal missing, between Crate and System FPGAs:
  - easily bypassed using spare track;
  - need to investigate cause.
- Crate and System FPGAs loaded successfully via JTAG.
- VME CPLD loaded successfully via JTAG.



• Some problems with VME write access. Investigating....

