CP VHDL Model at Birmingham

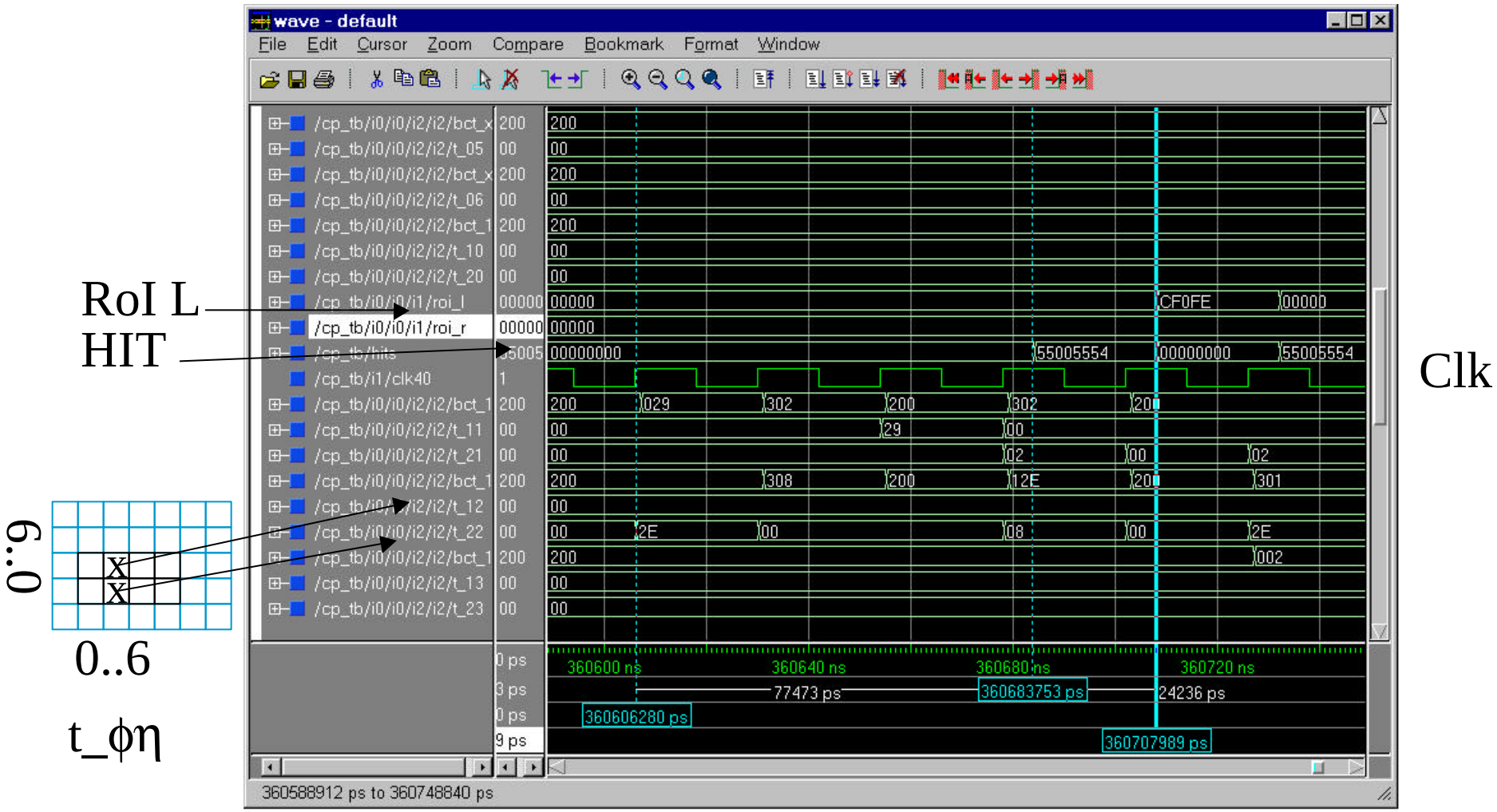
History

- Early this year B'ham people were interested to have the VHDL CP chip code
- Because the code is still not frozen, James issued a model of the code without access to the source code but…
- …still able to perform simulation and read internal signals
- Take a while to make it run locally: need new machine, updating/upgrading and write a local test bench

CP chip testbench

- Test bench already exist from previous simulation test but only at the start of the Serialiser
- B'ham test bench deals directly with the CP Chip input (108 pins of BCmux Data)
- It need in input 2 files generated by Steve:
  - Threshold data
  - BCmux data
- Test bench is working and results agree with Steve expected results
- Checked for a couple of values, thinking generated output file and cross checked all values

Latency


RoI L
HIT
Clk
6..0
0..6
t_ϕη
wave - default
File Edit Cursor Zoom Compare Bookmark Format Window
/cp_tb/i0/i0/i2/i2/bct_x
/cp_tb/i0/i0/i2/i2/t_05
/cp_tb/i0/i0/i2/i2/bct_x
/cp_tb/i0/i0/i2/i2/t_06
/cp_tb/i0/i0/i2/i2/bct_1
/cp_tb/i0/i0/i2/i2/t_10
/cp_tb/i0/i0/i2/i2/t_20
/cp_tb/i0/i0/i1/roi_l
/cp_tb/i0/i0/i1/roi_r
/cp_tb/hits
/cp_tb/i1/clk40
/cp_tb/i0/i0/i2/i2/bct_1
/cp_tb/i0/i0/i2/i2/t_11
/cp_tb/i0/i0/i2/i2/t_21
/cp_tb/i0/i0/i2/i2/bct_1
/cp_tb/i0/i0/i2/i2/t_12
/cp_tb/i0/i0/i2/i2/t_22
/cp_tb/i0/i0/i2/i2/bct_1
/cp_tb/i0/i0/i2/i2/t_13
/cp_tb/i0/i0/i2/i2/t_23
360600 ns
360640 ns
360680 ns
360720 ns
77473 ps
360683753 ps
24236 ps
360606280 ps
360707989 ps
360588912 ps to 360748840 ps

General Comments

- Latency: Total
  - BC D-Mux: 2 ticks 2
  - Cp algo: 3 ticks 5
  - RoI: 1 ticks 6
- Learn more bits of VHDL coding
- Have to change my VME access of my own VHDL code to match the CP protocol
- Takes 30 min to do the calibration, I.e simulated 358 μs

Next Steps

- Steve will generated more test vectors and investigate some interested cases
- Insert CP chip with ROC and Hit merger blocks
- Double check H/W testing
- debugging