Common Merger Module, status & test plans

- **Status at Last Meeting**
- **Status Now**
- **Schedule**

*"...puzzled but never quite defeated."*

CMM: Status at last meeting:

- Real-Time Path:
  - finished testing, no known problems

- Readout Path:
  - could not get G-Links on CMM to lock

- FPGA auto-configuration logic:
  - Problem fitting all required control functions into single CPLD
  - lacking software interface to load firmware via VME

CMM : Readout Tests

- Problem getting CMM G-links to lock:
    - bad clock due to missing termination (schematic error)
    - added termination; problem solved.
- Readout data transmitted to
    - DSS GIO Rx
    - CMM-CP ROD
- single & 3-slice data packets
- single & multiple L1As
- DSS:
    - slight oddity: final data word always appears in RAM twice. (DSS problem?)
- ROD:
    - data received successfully with correct format.
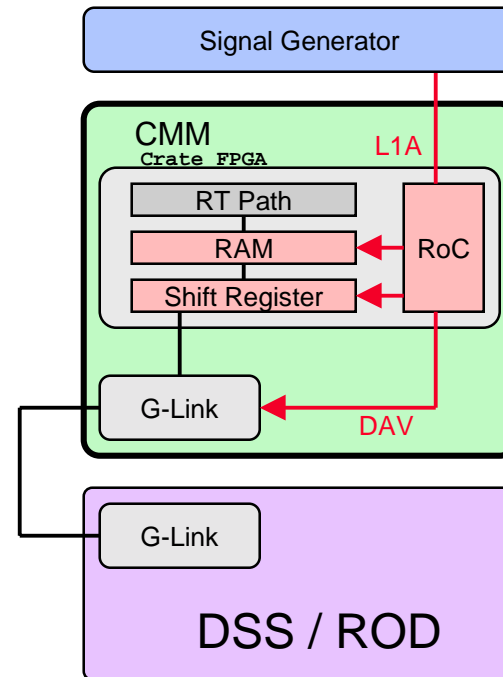
Tests with TTC Rx

- Took CMM to visit R1, where Bruce produced from TTC:
  - L1A
  - BCR
  - CLK40
  - CLK40Des1
  - CLK40Des2

- These are the only TTC signals we use
- Monitored via LEDs & scope probes
- All signals behaved as expected.
- Produced & observed phase shift between CLK40Des1 & CLK40Des2

- Found flaw in current design:
  - if TTC clock fails can't produce TTC reset without inserting jumper to switch to crystal oscillator.
  - Fix in next version.

FPGA Configuration Logic

Done:

- read & write data VME $\leftrightarrow$ FIFO
- load data FIFO $\rightarrow$ Flash
- read data VME $\leftarrow$ Flash
- erase Flash from VME
- load data Stag Programmer $\rightarrow$ Flash
- programme Flash $\rightarrow$ FPGA

- Now have single CPLD design that can control all of the above.
- Developing Labview Software to control downloading of firmware via VME.

To do:

- programme VME$\rightarrow$Flash $\rightarrow$FPGA
- load all 3 (System) Flash memories & test GeoAddr decoding
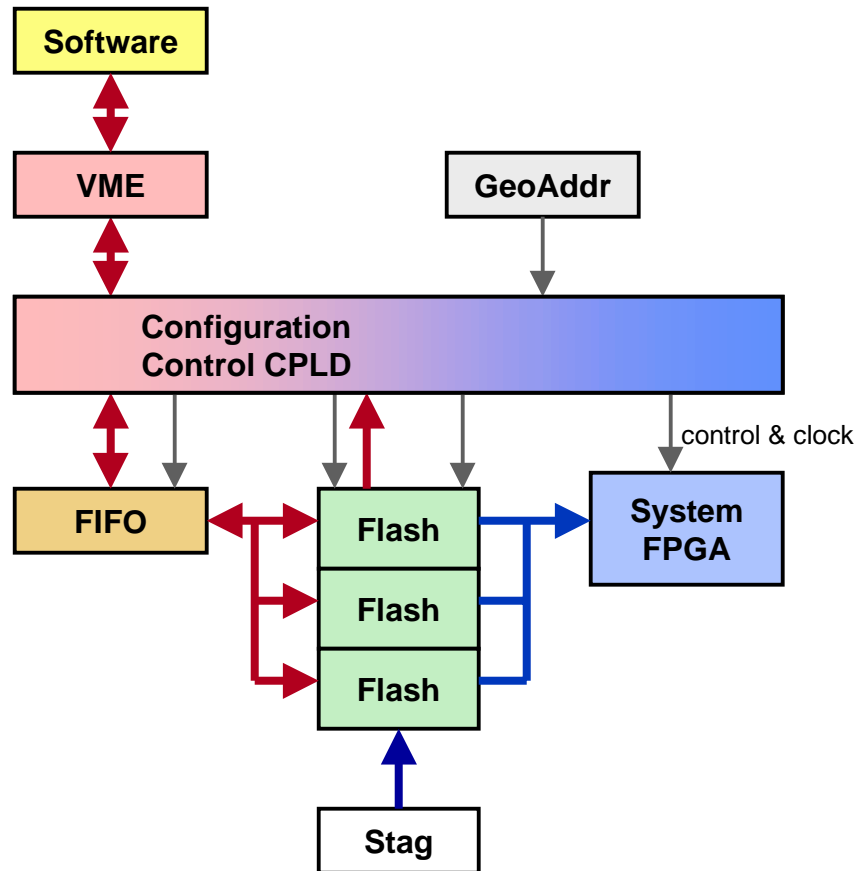
CMM: The Next Iteration

- Reviewed all problem reports generated by testing first CMM
  - Only JTAG error necessitates re-design
  - majority minor: missing termination, etc.

- Currently modifying schematics to correct all known errors
  - correct all errors above by making smallest possible change.

- Due to problems modifying VME interface & Config. Controller, decided to re-target:
  - was XC95288XL: 288 macrocells, 6400 gates
  - now XCR3384XL: 384 macrocells, 9000 gates

- Schedule: submit to Drawing Office beginning of January 2003.

Summary

- Planned CMM tests almost finished
  - final test of auto-config. logic remains to be done.
  - working on this in parallel with...

- Preparing schematics for next iteration of CMM design

- Plan to begin board layout 2nd January 2003.

- On schedule to have CMMs ready for sub-system tests March 2003.