CPM Testing

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Serialiser Chip:LVDS path

- LVDS receiver:
  - LVDS signals locked correctly
  - Was working earlier but lock signal was mishandled inside serialiser
- Serialiser:
  - F/W correction: mishandling corrected and …
  - Data generated in DSS playback memory correctly recovered inside SRL playback memories
  - Minor correction needed to generate init_sync on board, but synchornisation could be performed easily by hand
- To do:
  - Soaking test
  - investigates other channels, so far 1 SRL tested

Hit Merger

- With the help of extender and logical analyser:
  - Access to real time data path
  - Bit correctly generated and in right order
  - Glitch appear from time to time, F/W problems?

Readout Controller DAQ & Roi

- With the help of logical analyser:
  - Check validity of Data, DAV signal and slices : working correctly
- To be done:
  - Feeding into Glink DR available in the lab:
    - F/W could be modified to generate a pseudo random pattern and be recovered in Glink sink card: soak test

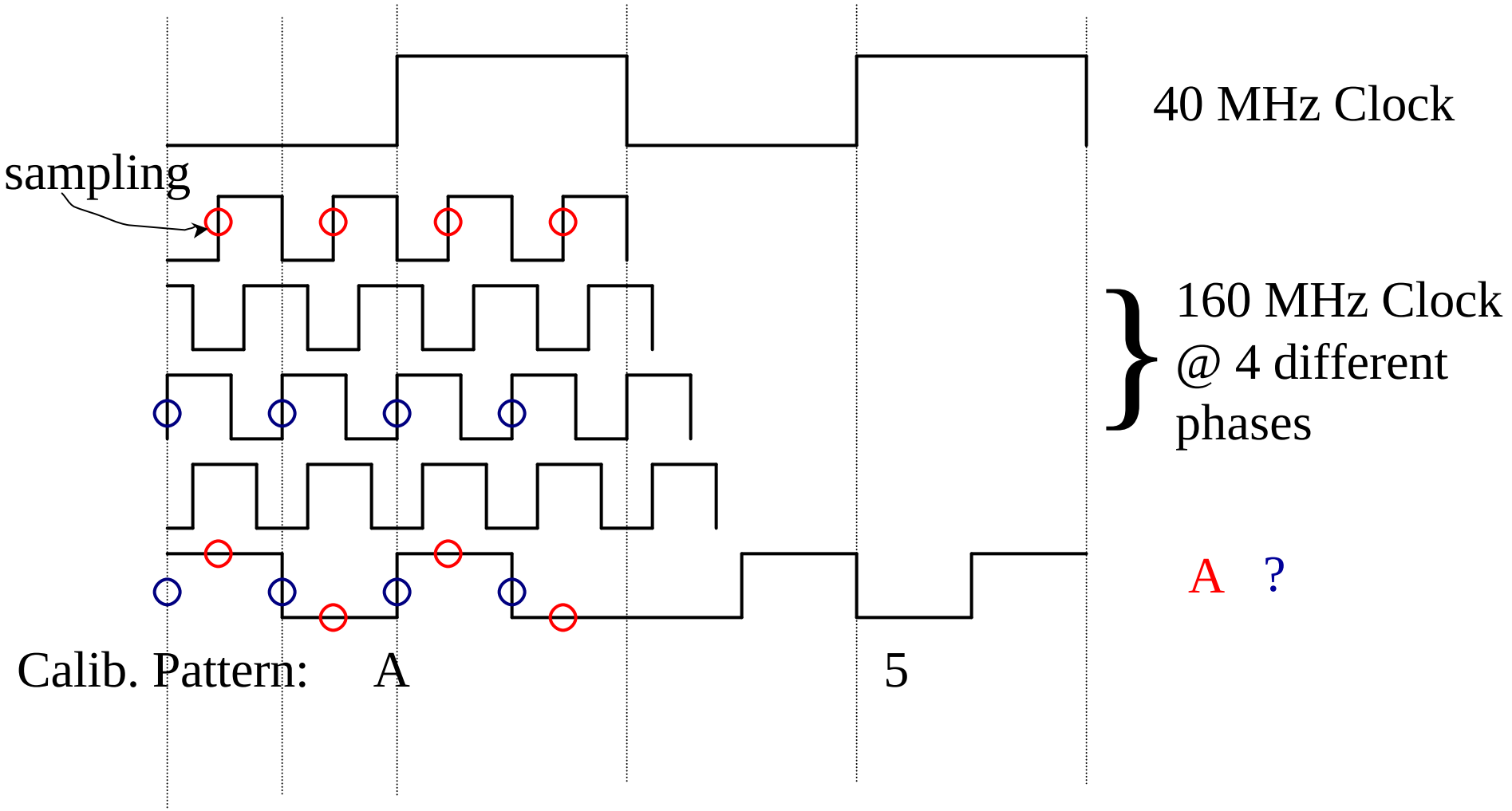
CP chip F/W investigations

- Data are corrupted on 2 or 3 channels from time to time
- James and Ian came with Chipscope (4) to investigate the problem
- Problem coming from the serialiser was eliminated
- Problem appear to be in the calibration process

CP Chip F/W investigations

- Calibration process problems:
  - Channels locked but the process of calibration was odd
  - Channels refused to lock
- The way the calibration process works:
  - Up to 4 attempts of calibration are performed on each channel
  - Expect channel to lock on the first attempt
  - Corrupted data appear on channel locking after several attempts
- F/W investigation: see next slides->

CP chip : Calibration Process

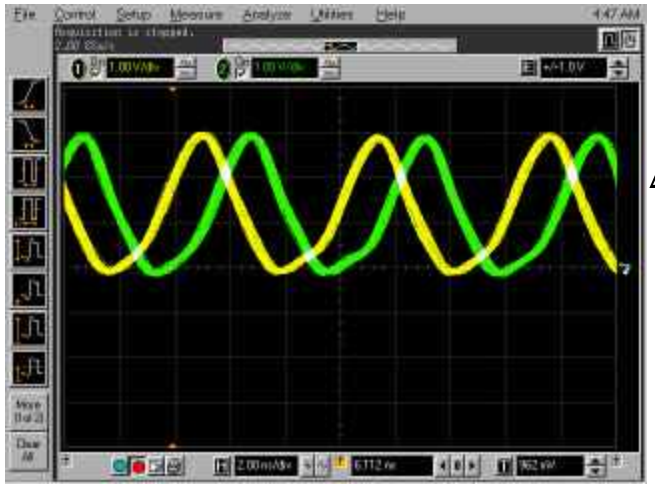


CP chip F/W investigations

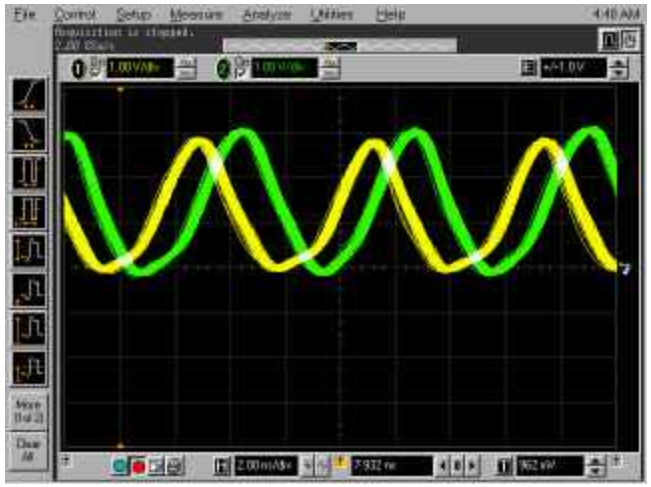
- Several F/Ws have been written by James to understand misbehavior :
  - One F/W generate internally the calibration pattern: expect 100% of pins locked but only 92% did
  - One F/W output 160 MHz signal generated by the Fpga for 4 different phases, and used by the calibration process
- Shape of waveform of the 160 MHz is not very nice, and the relative phase between them not constant:
  - But agree with simulation!
  - Need a better jitter and precision of 1.65ns apart
- Solution:
  - Meeting in January: tutorial on calibration process
  - By-pass calibration process, do it with S/W (relative input signals better than 1 ns)
  - Upgrade Fpga?

90^0 phase difference between the 4 160 MHz signals

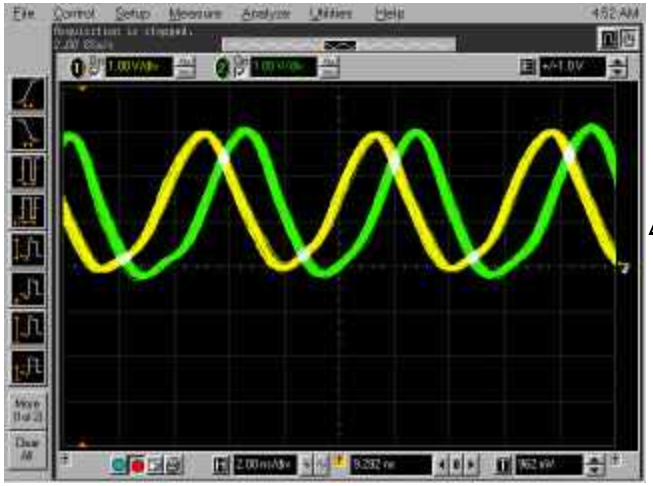
Trigger is on 40 MHz clock



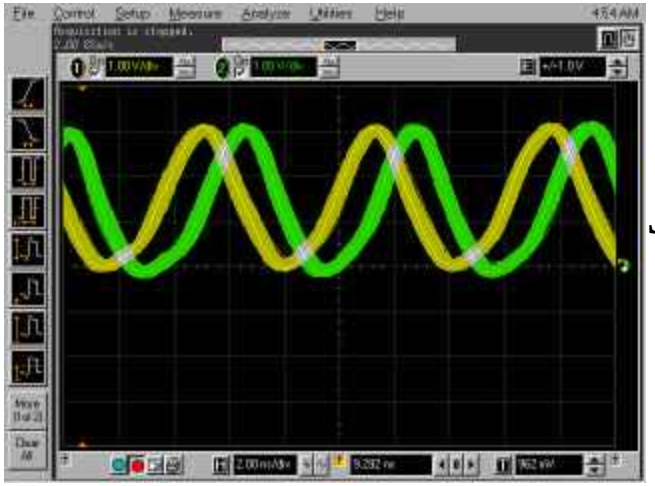
Δϕ:1.6 ns



Δϕ:1.ns



Δϕ:1.5.ns



Jitter:450ps

CPM Services - Software

- Not much unfortunately!
  - Used Hdmc successfully without the segmentation fault
- To be done
  - Run Controller integration
  - New database format
  - Change in Fpga downloading
  - Integration with external modules such as DSS

Conclusion

- CPM is almost fully working:
  - CP chip F/W show some problems: delay???
  - Need testing all LVDS inputs, tedious: 1 day
  - I2C access with new TTCdec card: 2 days
  - CAN bus: 1 day
  - Soaking tests:
    - more LVDS signals needed
    - ROC F/W to be modified
- S/W:
  - Works to be done: 1 student available for January and February
- 2nd CPM, once assembled:
  - Testing algorithm and backplane, with help of GIOs and more DSSs