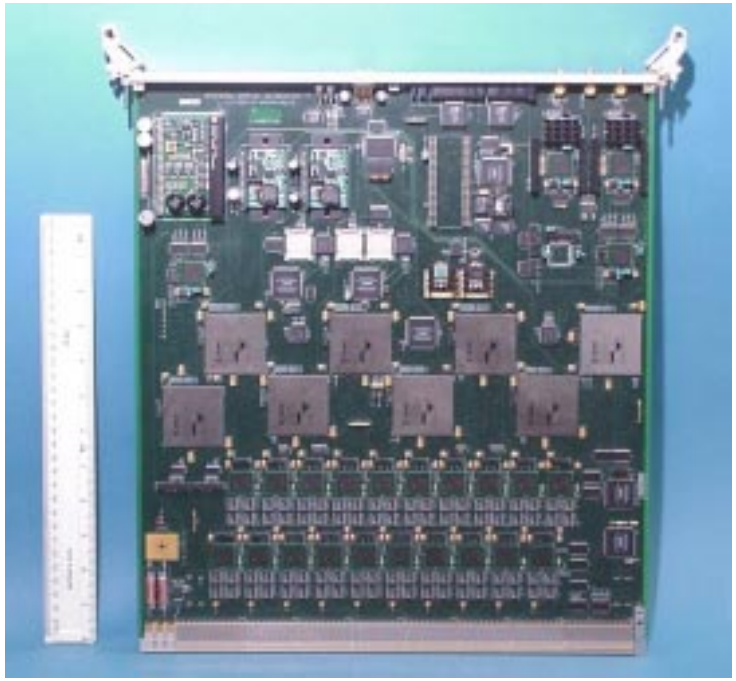
CPM Prototype Hardware Status

- Extender
- 160Mb/s signals
- 160Mb/s links
- Assembly of #2
- Summary



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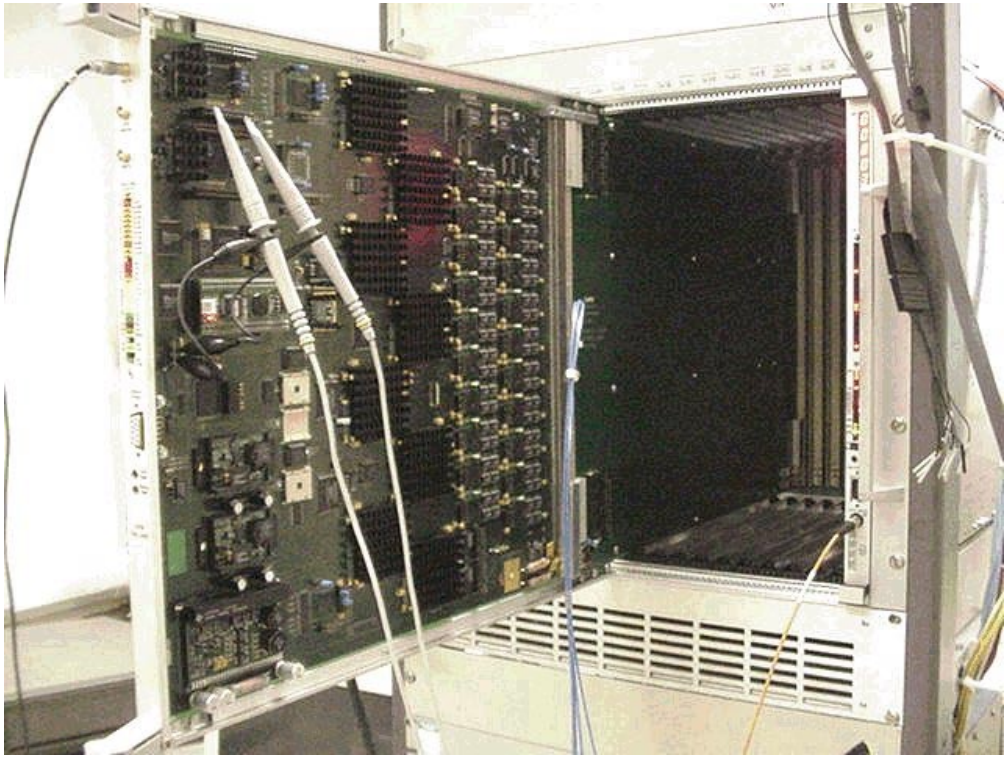
Extender

Now in use - better access to both sides of module.



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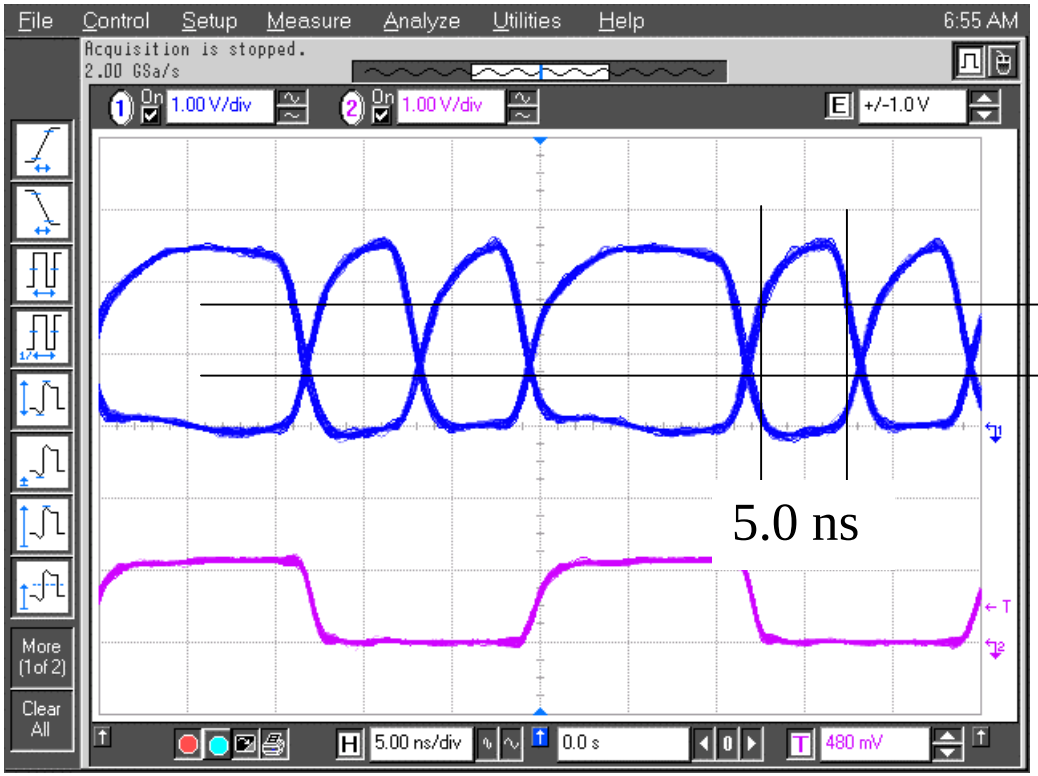
160 Mb/s Links

Typical CP chip input , direct from Serialiser (series term.):



1.7V V_{ih} CMOS2 thresholds

0.7V V_{il}

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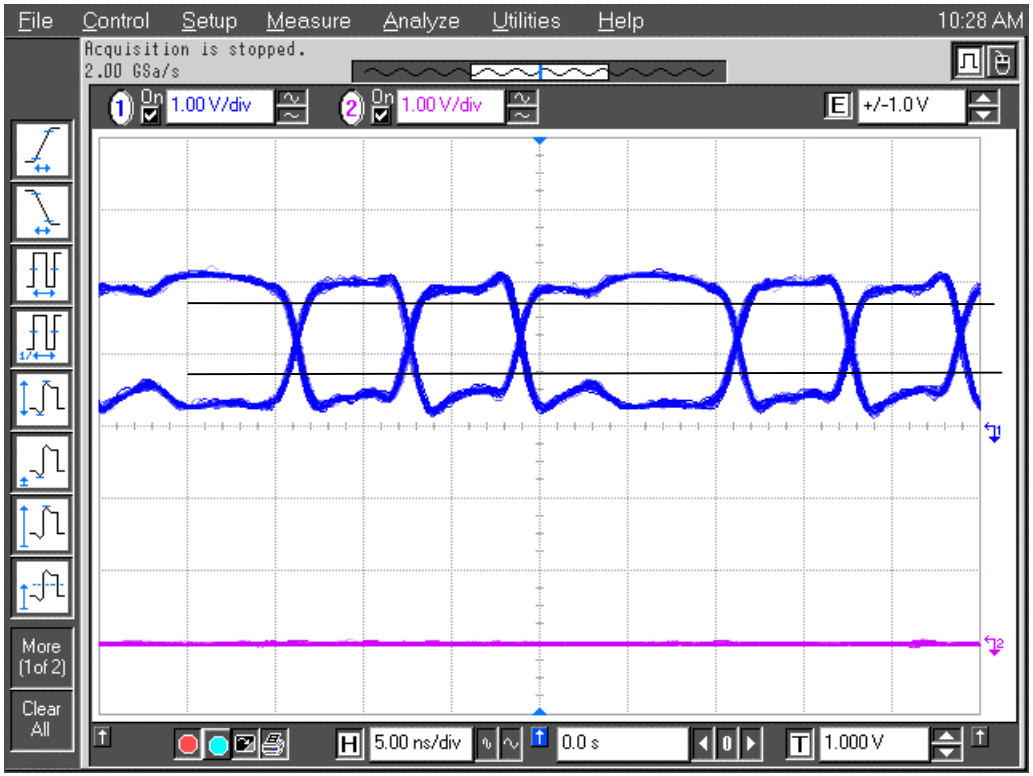
160Mb/s CP Inputs via backplane (parallel terminated)

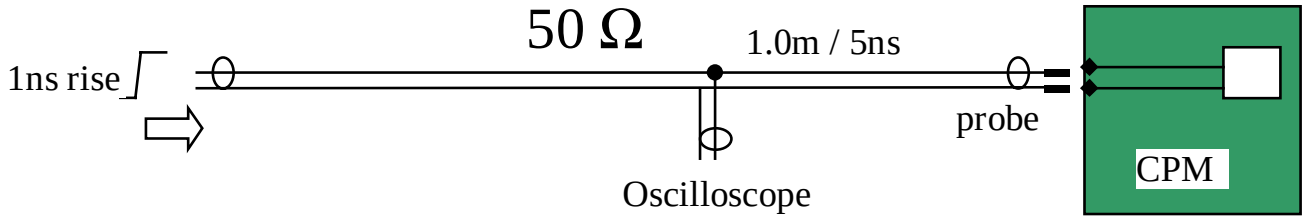


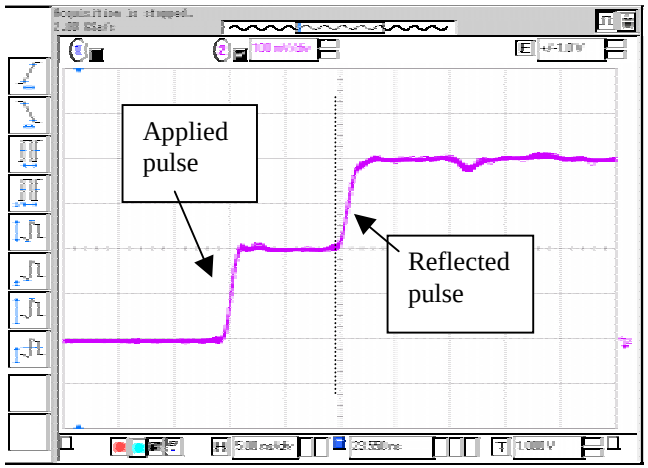
Poor voltage margins caused by:

- Reflections
- Attenuation
- Crosstalk

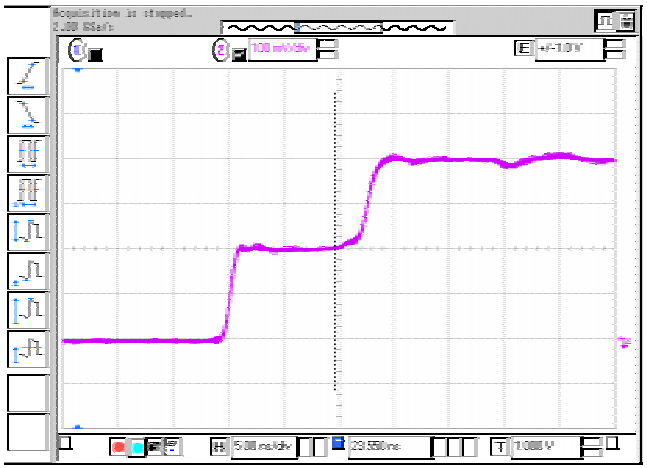
- Reflections

Time Domain Reflectometry (TDR) on CPM (Unpowered)



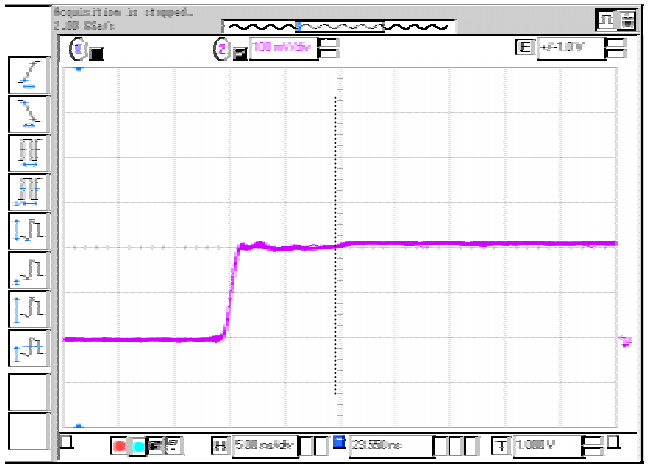


Open-circuit

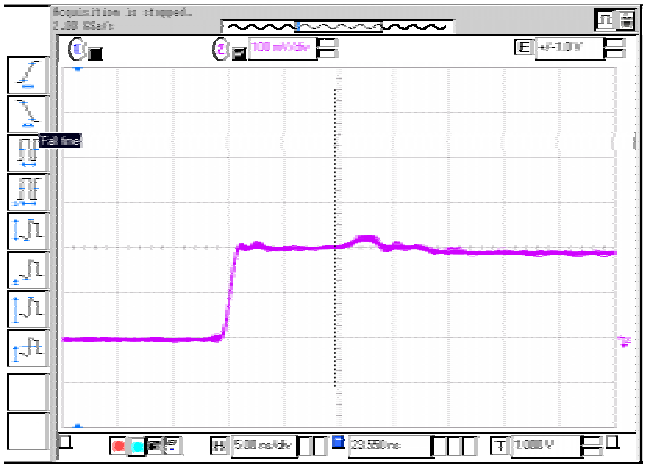


Backplane to Serialiser Output

TDR continued:



56 ohm resistor



Backplane input to 3 CP FPGAs

Impedance mismatch appears acceptable.

- Signal Attenuation

Tracks are 3 thou wide , with 1/2 oz / ft2 copper.

5 - 6 Ω track resistance, from connector to last CP FPGA.

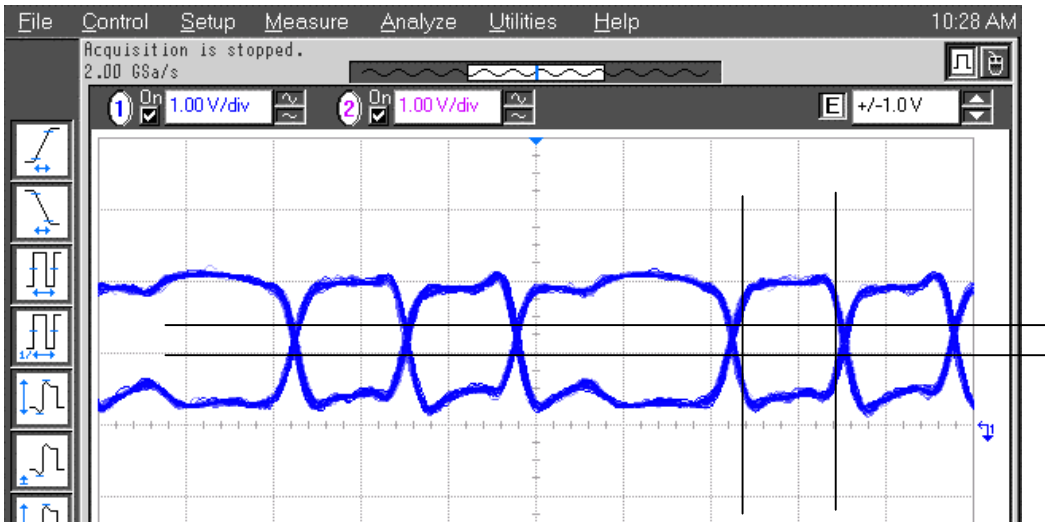
With 56 Ω termination → 10% attenuation.

- Crosstalk

To be investigated.

What can be improved? PCB ?

The FPGA has inputs options that have better defined thresholds:



V_{ref} + 0.2v CTT / SSTL2

V_{ref} - 0.2v I/O Standards

... but these options need 30 Vref inputs which are unconnected.

Not possible on the present CPM.

160 MB/s links

CP FPGA Data timing calibration not working

Problems vary with CP FPGA Firmware version.

Are our devices fast enough? (Yes)

Do we need to change the design?

XILINX®

3 (v1.2) January 6, 2001

Multi-Channel 622 Mb/s LVDS Data Transfer for Virtex-E Devices

Author: Brian Von Herzen, Ph.D. & Jon Brunetti

nary

Virtex™-E devices provide dedicated on-chip differential receivers between adjacent user I/O pins, which are ideal for receiving LVDS signals at speeds of up to 622 Mb/s in the –7 speed grade. This application note describes how to design a high-speed, low-voltage differential signaling (LVDS) transmitter and receiver in a Virtex-E FPGA suitable for point-to-point data transmission at a data rate of 622 Mb/s.

Table 2: **IOB Input Switching Characteristics** ***(Continued)***

			Speed Grade[1]				
Description[2]	**Symbol**	**Device**	**Min[3]**	**-8**	**-7**	**-6**	**Units**
Sequential Delays							
Clock CLK to output IQ	T_{IOCKIQ}	All	0.18	0.4	0.7	0.7	ns, max
Setup and Hold Times with respect to Clock at IOB Input Register							
Pad, no delay	T_{IOPICK}/ T_{IOICKP}	All	0.69 / 0	1.3 / 0	1.4 / 0	1.5 / 0	ns, min

CP FPGA -6

Assembly of #2

?

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Summary

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