JEM-1

Final Design Review

Birmingham

11-12 December 2002

Review Panel – Eric, Tony, Steve, Richard

(plus further useful comments from Murrough and Norman)

Agenda

- **Purpose of Review – general issues to establish:**
  - **What lessons have been learnt from JEM-0 to inform new design?**
  - **Have all necessary performance features been included?**
  - **Is design sufficiently compatible with CPM in regard to online software control?**
  - **Decide which design variant to pursue for JEM-1**
- **Outline of proposed changes between JEM-0 and JEM-1**
- **Discussion of responses to reviewers' written comments and queries**

Other specific issues for discussion:

- Data synchronisation schemes in Input Processors
- Clock distribution scheme
- DAQ and RoI readout sequencing
- Data formats to RODs
- FPGA configuration architecture
- Playback and Spy memory organisation
- Use of daughter-card construction for Input Processors
- Use of TTCdec and Fujitsu CANbus controller design from CPM
- Possible timescales and costs

Proposed Modifications – JEM0 → JEM1

Replace de-serialisers by compatible 6-channel devices with Boundary Scan facility. Allow for use of redundant 7th channel – reduces the need for re-work of the de-serialiser BGAs

Replace 11 input FPGAs *(8-channels each)* by 4 Virtex-II chips

Use 24-channel input daughter cards – reduces board routing complexity and improves serviceability

Make input FPGA control path *(VME)* compatible to the one used on JEM0.0 main processor *(point-to-point, no ring bus)* – minimises number of board layers

Widen on-board VME control paths slightly

Replace main processor by larger Virtex-II device in 1.27mm BGA package

Use 1.5V signals where possible *(previously 2.5V)* – reduces noise/crosstalk

Use internal source termination *(DCI)* on all signals *(was discrete source termination on JEM-0)* – removes large number of discrete resistors

Replace all CPLDs by a single FPGA configured from flash memory

Move TTC control and clock mirror into ROC and provide full access to TTCrx

Widen TTC/DAQ paths to the processors slightly

Add parallel flash memory for processor configuration *(CPM style)*

Make CAN hardware identical to CPM *(Fujitsu)*

Preliminary Conclusions

- **Recommend that no further JEM-0 modules be made – first two to be used for initial sub-slice tests only**
- **Recommend that all major design upgrades be adopted – work on full-spec JEM-1 should proceed as fast as possible, with two modules to replace JEM-0s in Slice Tests**
- **Specific recommendations:**
  - **Use daughter-cards for Input Processors, with high-density *(0.5mm)* differential-pair*Samtec* connectors, to reduce risks of main pcb construction**
  - **Use common TTCdec design – also possibly with high-density *Samtec* connectors**
  - **Move to boundary-scannable 6-channel LVDS deserialisers, located on input d-cs**
  - **Allow for up to one full BC of skew on input signals**
  - **Ensure agreement between data formats of DAQ/RoI outputs and ROD inputs**
  - **Ensure that channel labelling and connectivity from PPMs is correct and unambiguous**
  - **Use CP-style *Fujitsu* CANbus controller**
  - **Use of front-panel indicators to match those on CPM as far as practicable**
  - **Provide U-frame mechanical stiffeners around main pcb**